At-Speed test Prominence

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Abstract**—** *With the remarkable scaling down of technology, test engineers are encountered with new challenges. With the reduction technology moving down to Deep Submicron level, the digital designs are moving closer to the probability of defects related to time. The traditional Stuck-at tests and IDDQ tests can no more detect few distinctive faults which may be occurring due to issues related to timing of the signal. The defect spectrum is thus broadened by the inclusion of other types of faults such as high impedance shorts, in-line resistance, and cross-talk between signals. This paper proposes the use of At-Speed test which is better suited to detect the new types of failures that occur in a digital circuit due to its complex design. The use of At-speed test ensures the timing reliability of the chip after manufacturing thereby reducing DPM (Defect per million) rate. At-speed tests when added with the traditional stuck-at tests, guarantees maximum fault coverage and reduced DPM rates (@30 to 70%). Though At-speed testing is not a new concept and few ASIC vendors have been using this, they have been using functional test patterns to create them which are a very tedious and time consuming routine. Diagnosing the failure source also becomes difficult with the failure of functional patterns. This paper discusses about the fault models provided by industries leading ATPG tools that targets the At-speed failure.*

Keywords**—** ***At-Speed test, functional test patterns, fault coverage, Stuck-At-Test, IDDQ Tests.***

I. INTRODUCTION

A physical defect within a circuit or a system is termed as Fault. A fault may cause a system failure or sometimes may not affect the system at all and goes unnoticeable. A fault that results in an incorrect state of the circuit generates an Error. This error deviates the entire system to work as per its specified design and the design fails in its functionality. This is called the failure of the system. Hence the failure of a system is caused by an error in the circuit and the root cause of this error may be a small fault in the smaller abstraction levels of the circuit. Thus identifying and fixing every single fault is very important. A scan test using Automatic Test Pattern Generation (ATPG) is done which detects any manufacturing defects in the circuit. The Test operates on two modes, A shift mode and Capture mode. In the shift mode, all sequential elements are connected as shift registers. This mode is used to control the circuit and observe the result. Whereas in the capture mode, the values stored in the sequential elements are propagated from the source and through the functional logic to the sink. Defects are broadly categorized as follows:

a) Functional defects

- Circuit open
- Circuit Shorts

b) IDDQ defects

- CMOS Stuck-on
- CMOS Stuck-open
- Bridging

c) At-Speed defects

- Slow Transistors
- Resistive Bridges

1.1 Stuck at Fault Model

This comes under functional defects which are caused due to shorts and opens in the device interconnects. This model assumes only one faulty input for every single gate. This model alone cannot cover several other kinds of defects present in the circuit.

1.2 Bridging Fault model

In this model, it is assumed that two signals are connected together, when they should not be. This kind of fault results in Wired-and or wired-or logic. Bridging to VDD or VSS becomes analogous to stuck-at fault model.

1.3 Transistor Faults

This model generalizes defects related to CMOS logic gates and comes under IDDQ defects. At transistor level, a transistor may be stuck open or stuck-short. Stuck-short assumes the transistor to be always conducting and stuck-open condition assumes the transistor to be always non-conducting. The IDDQ test measures the quiescent supply current to detect few failures which are not easily found by functional testing methods.

1.4 Open Fault model

In this model, a wire is assumed to be broken and one or more inputs are assumed to be disconnected from the primary outputs.

1.5 Transition Delay Fault Model

The fault caused due to rise and fall times are called Transition delays, accordingly there are two types of transition faults which are **Slow to Rise** and **Slow to fall.** A stuck-at-0 for slow to rise and a stuck-at-1 for slow to fall may be used. This approach however may not be able to detect accumulated delays throughout a large circuit.

1.6 At-Speed test

This model, which is also the prime area of the study detects the delays introduced by resistive defects. At-speed test is considered a must to maintain acceptable DPPM rates in any nanometre design.

There are two types of at-speed fault models which are widely accepted in Industry today. They are a) The Path delay model and b) The Transition delay model. They both work by generating scan pattern unlike stuck-at-fault model which is a static testing method. This testing consists of two parts, first part launches a logic transition and the second part captures the response. If the transition fails to update within the capture time, we say that the test is failed and the circuit is having At-speed defect.

An example is present below to show how the At-speed test works:

Goal : Propagation from 0 to 1 (Rising Transition)

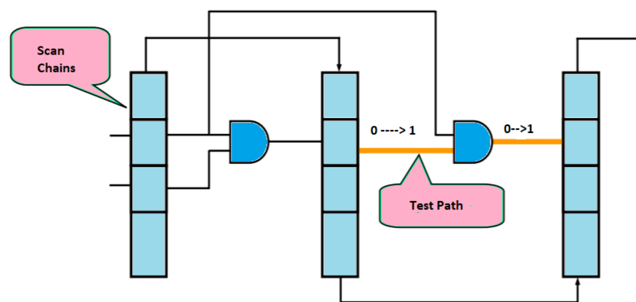

FIG 1: Goal: detect fault from 0 to 1 i.e. in a Rising transition

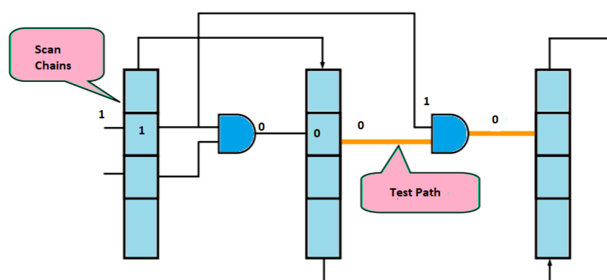

FIG. 2: Define initial values for path sensitization

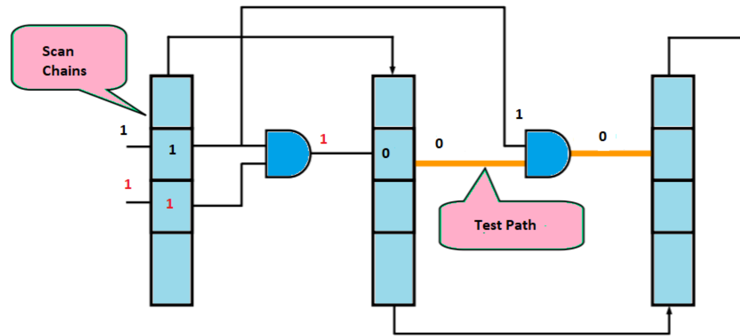

FIG. 3: Define values for launch event (scan chain values are known now).

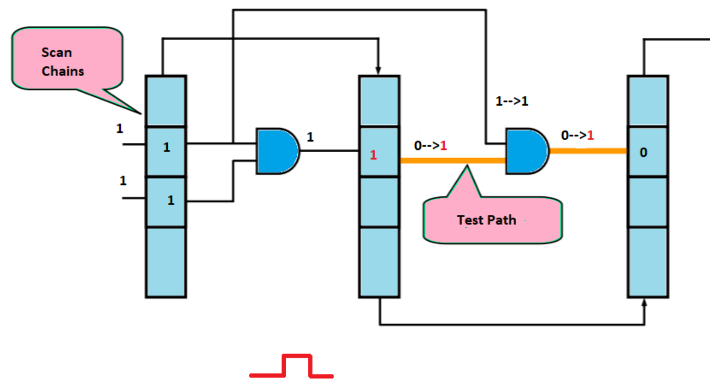

FIG. 4 : Pulse Clock to launch (Value gets changed and starts propagating).

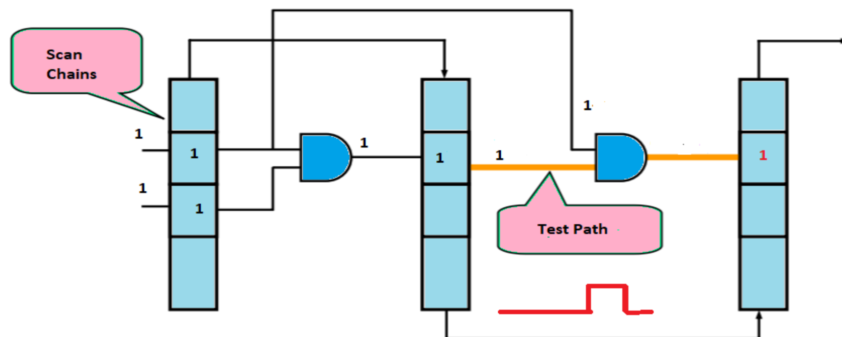

FIG. 5: Pulse Clock to Capture (Value gets propagated)

II. PATH DELAY FAULT MODEL (PDFM)

This model is used to capture small as well as large delay defects which may be present along a path in the circuit. It is preferred to generate tests only for few critical paths as there are enormous test paths in the circuit design and test generation for all the paths is impossible. Only test for critical paths are generated to ensure that the timing behaviour of the signals are working as per the golden reference (i.e. as desired). Path delay fault, models manufacturing defects that can causes cumulative delays along the critical path of the design. The critical path in a design can be identified by using a static timing analysis tool. Test patterns for faults along these critical paths are generated by an ATPG tool. The path delay testing typically is done between start and end of scan cells. Path delay patterns helps to verify the device's operating frequency and sometimes also for speed binning. By manipulating the launch-capture sequences, device's can be tested for various speeds.

2.1 Path Delay test implementation

1. A list of all critical path is generated by a Static time Analysis tool.
2. These paths are given as input to FastScan (ATPG tool)

3. ATPG tool also checks the integrity of the path as sometimes STA also reports some false path.
4. After identifying all real paths, the ATPG tool generates test patterns for those paths.
5. A fault list is generated which contains two faults per path, Slow to rise and slow to fall defects.
6. The ATPG tool provides a test coverage number that includes only the loaded path and not all paths in the design.

III. TRANSITION DELAY FAULT MODEL

The faults caused due to Rise and fall time of the signals are called transition delay faults. There is a finite time between the applied input and output response. This area is prone to create faults in the absence of proper time for the settlement of signals. As seen earlier in (2) that there are two kinds of transition faults slow to rise and slow to fall in path delay, but this method is confined to the supplied critical paths unlike transition delay testing which automatically chooses small paths in the design that include the targeted fault location. There are again two kinds of transition tests a) Launch-Off-Shift and b) Broadside. These are described in the below section:

3.1 Launch-Off-Shift

LOS patterns are shown in fig. 6. This approach involves launching during the last shift of scan chain loading. The circuit is then placed to capture mode within no time i.e., the scan enable signal should have the transition very quickly after the last shift of functional frequency so that the logic is allowed to settle before the capture clock occurs. The Scan enable signal should be routed as a high frequency signal. This approach gives highest test coverage and results in faster ATPG run time.

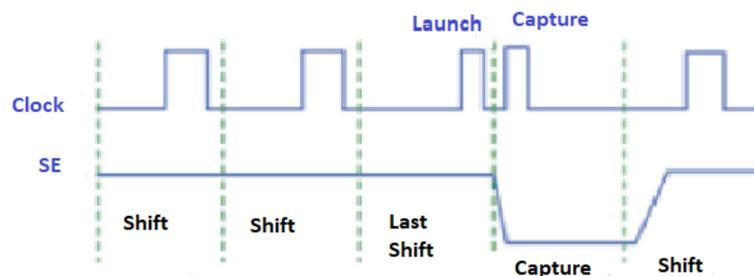

FIG.6: Launch off shift transition patterns.

3.2 Broadside (Launch on Capture)

This approach launches the transition in the functional mode. Before that, first the entire scan data shifting is done in test mode. Later two at-speed clocks are pulsed for launch and Capture in the functional mode. After capturing the values, the data is shifted out slowly in the test mode. This approach is most accepted by many companies for reasons mentioned in (4).

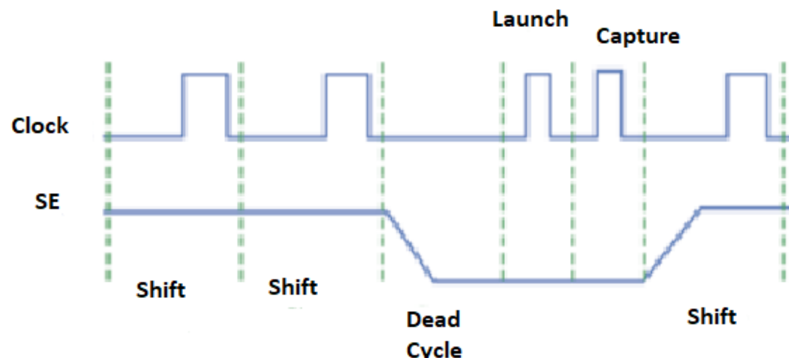

FIG.7 - Broadside (Launch on Capture) transition patterns

IV. LOC / LOS LIMITATIONS AND STRENGTHS

ATPG is much easier with LOS as compared to broadside patterns. LOS achieves higher coverage and escalates the ATPG run time. Even though Broadside approach is more commonly used as compared to LOS. The main reason must be the

difficulty in changing the circuit from shift mode to functional/capture mode between the last shift and functional clock pulse. Another concern with LOS is that it may end up testing non-functional logic at-speed thus resulting in increased yield loss. On the other hand broadside pattern launches the transition in the functional mode of operation thus propagating transitions along real functional paths. In broadside approach, it is sometime required to add some extra cycle which is called as dead cycle to ensure that Scan enable settles completely.

V. OTHER APPROACHES

Manufacturers are continuously on a hunt to improve the efficiency of At-speed scan testing. An approach called Timing aware is used which targets small delay defects. Here each fault is tested by propagating the transition down as slow as possible.

Also few novel techniques like pipelined scan enable is in use that makes LOS more feasible. The pipelined Scan enable adds additional test logic to the design and triggers a change within the local scan enable thus removing the difficult task of treating scan enable as a global clock.

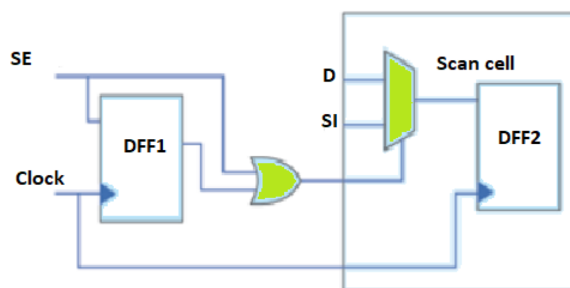

FIG 8 – Pipelined Scan enable

VI. CONCLUSION

We have several other new genres of defect arising due to nanometre process. Thus using only conventional testing approaches may put companies into high risk of increase in DPM levels. At-speed testing is the best solution. LOS and LOC approaches and their pros and cons are discussed. With the help of pipelined scan enable, the difficulties in LOS approach are rendered thus allowing users to assess the trade-offs between the two approaches and decide and plan the best solution for them.

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