Comparative Study of Sense Amplifiers for SRAM

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Abstract— *This paper presents the comparative study of different type of sense amplifiers. These sense amplifiers are voltage-mode sense amplifier (VMSA) and Charge transfer sense amplifiers (CTSA). The first objective of this research work is to design the sense amplifier and the next objective is to compare and identify which design has better performance in term of power and speed. Sense amplifiers are one of the most essential circuits in the CMOS memories that plays an important role to reduce the overall sensing delay and voltage. Previous voltage mode sense amplifiers sense the voltage difference at bit and bit lines bar but as the memory size increase the capacitances of bit line and date line also increases. The tools used for simulation is TANNER EDA for layout using 90nm technology. The results show that the CTSA has higher speed with lower delay and low power dissipation than VMSA. But cell size of VMSA in comparison with CTMA is smaller. CTSA is more suitable for high speed performance and low power circuitry and VMSA is best suited for stability and smaller design.*

Keywords— 6T SRAM, Voltage mode sense amplifier (VMSA), Charge transfer sense amplifier (CTSA).

I. INTRODUCTION

SRAM stand for Static Random Access Memory, a nonvolatile memory that can store the information as long as the power is applied. The sense amplifier operated only when stored data is read from memory. Sense amplifier (SA) is used to detect the very small difference voltage at bit-lines and amplify the signals to its full digital voltage swing before the signals are fully charged or discharged. This situation causes the time taken to read the content of memory is shorten since the circuitry does not requires to wait until the signals getting fully charged or discharged to determine either it is '1' or '0'. The small spark or glitch at both bit-lines may determine its state. So the memory may take it quickly either as 'I' or '0' rather than trying to calculate or wait for its voltage full swing level, thus saves time in read operation into memory.

In this paper the sense amplifiers are selected is conventional voltage sense amplifiers and charge transfer sense amplifiers. These sense amplifiers are simulated at 90nm technology scale. At this technology sense amplifiers is compared on the basis of sensing delay and power consumption at different voltages.

The organization of this paper is done in following manner i.e. initially a brief explanation of 6T SRAM and conventional sense amplifiers are done. After that comparison of both the sense amplifiers is done with graph.

1.1 6T Sram Working

SRAM consist of six transistors in which four transistors i.e. two cross coupled invertors as shown in figure1. Two NMOS transistors which are known as access transistors were connected to this cross coupled structure and bit-lines (i.e. Q & Q_b). These access transistors are operated by the wordline (WL). Static RAM operation is done in three modes i.e. Standby, Read & write mode. In Standby mode the information stored previously in SRAM cell is remains indefinitely as long as power supply is there. So wordline is grounded during standby mode. In read operation first of all bit-lines are pre-charged to Vdd and then wordline (WL) is selected to turn on the access transistor. These access transistors connect the bit-lines to the memory cell.

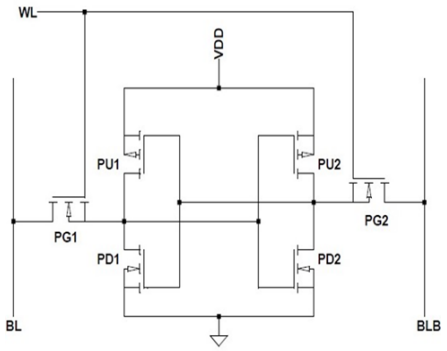

FIGURE 1: 6T SRAM

Memory storing a logic value '0' i.e. (a low voltage), therefore the bit-line is discharged through pull-down transistor & access transistor so that the differential voltage is developed between bit-lines. This differential voltage is sensed by the sense amplifier to show the information stored in cell. This difference in voltage should be large enough to detect but not extremely large, otherwise the state of the invertor will be flipped. Same as SRAM cell reading operation, the two bit-lines are pre-charged to VDD in a write operation. The address decoder enables the word line (WL) to turned on the access transistor. Figure shows a 6T SRAM cell's initial condition before a write operation, where the cell initially stored logic "1" at node Q (HIGH) and is written with a logic "0" (Node HIGH is pulled down to ground).

1.2 Sense Amplifiers

Sense amplifiers are the most essential circuit of SRAM which detect the voltage different between the bit-lines and show which data value stored in the memory cell. In this paper we discuss two type of sense amplifiers i.e. Voltage Mode sense amplifiers and Charge Transfer sense amplifier.

1.3 Voltage Mode Sense Amplifier

The operation of voltage mode sense amplifier is based on the differential voltage developed by the bit-lines. The circuit consists of cross coupled inverters that converts the bit-line voltage difference at their input to full swing output figure 2 shows the voltage mode sense amplifier circuit implementation. BL and BLB inputs are coupled to the column bit-lines of the cell. The inverters are form by P6-N1 and P7-N2 that convert the differential voltage on the bit-lines to a full-swing at the output. The precharge circuitry is formed by P3, P4 and P5 which is used to precharge the internal nodes X, $\overline{X}$ of this circuit through the bit-lines. The memory cell is connected to the sense amplifier by P1, P2 while to enable the sense amplifier N3 is used. The internal nodes of the sense amplifier is isolated from the external load by output inverters. The operation of voltage mode sense amplifier is done in two phases. In the first phase i.e. pre charge phase, the PCH is kept active low so that bit-lines and the nodes X and $\overline{X}$ are pre-charged high. During the evaluation phase, sense amplifier is connected to the memory cell by pulled down the select-line (SEL). A voltage difference is developed between bit-lines BL and BLB due to the stored data in memory cell. If the data stored in the memory cell is a '1', voltage across BLB decreases slightly and if the stored data in memory cell a '0', voltage across BL decreases slightly. Once the required differential voltage has been developed between bit-lines, EN is pulled high to enable the sense amplifier. Differential discharging of the bit-lines capacitance is used by the VMSA for sensing the voltage difference and converts this differential voltage at its inputs to a full swing at the outputs.

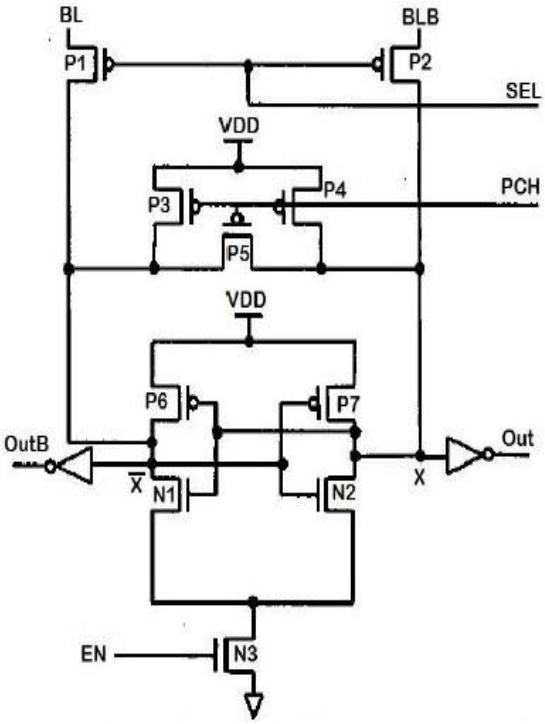

FIGURE 2: VOLTAGE MODE SENSE AMPLIFIER

1.4 Charge Transfer Sense Amplifier

The basic function of Charge Transfer Sense Amplifier is depends upon the charge redistribution from high bit-line capacitance to the low capacitance of the nodes X and $\overline{X}$ as shown in figure 3. The high speed operation of CTSA is due to to this charger distribution [5][6]. The circuit has two parts in which P6, P9, N1 & P7, P10, N2 form common gate cascade with PMOS P6 and P7 biased at V_o. In the other part P12, P13, N3 and N4 form the cross-coupled inverters[7]. CTSA is operated in two phase. In the pre-charge phase, high pre-charging of the bit-lines and all the intermediate nodes (A, B, C & D) is done. By keeping EN high the output of the common-gate amplifier (X and $\overline{X}$) is pre discharged low. In the evaluation phase, PCH is kept high and SEL input is grounded to select a column. By dragging EN low CTSA is enabled. Assume the bit-line BLB is going low. As the voltage of the BLB goes immediate $V_o + |V_{TP}|$, P6 goes into sub-threshold region of operation avoiding the output node from getting charged. However, the other bit-line BL remains high and charges the output node X to high.

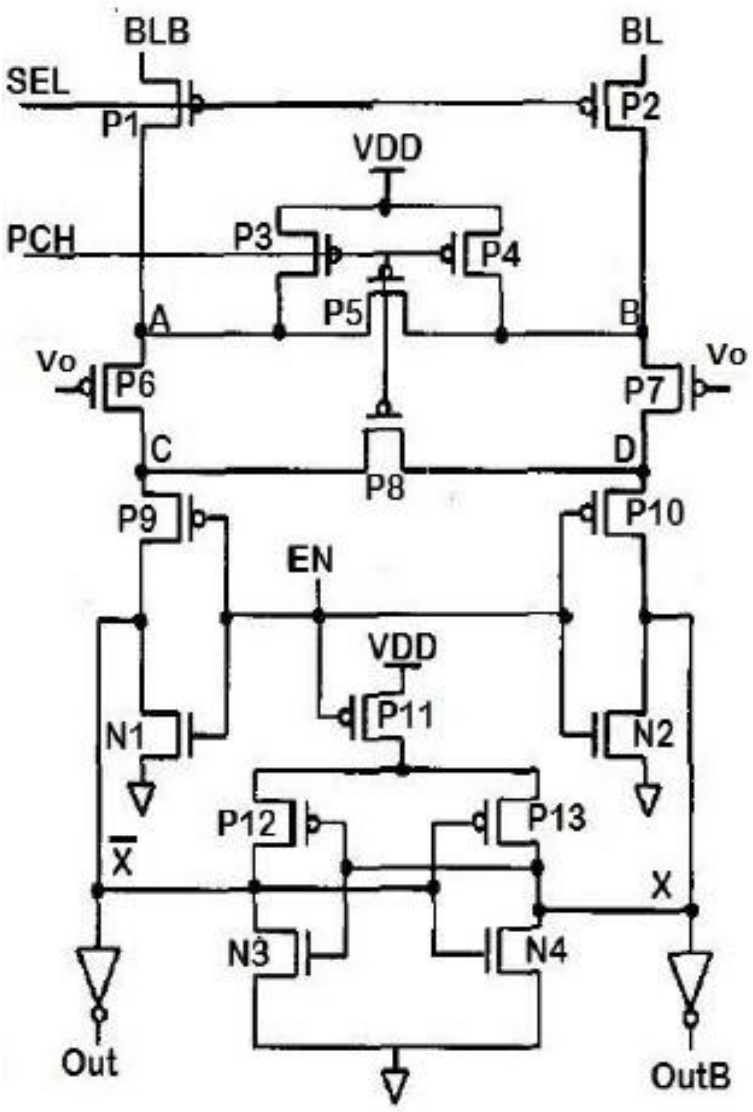

FIGURE 3: CHARGE TRANSFER SENSE AMPLIFIER

II. SIMULATION RESULTS

The sense amplifiers given in figure 2 and figure 3 have been designed and analyzed on the basis of average power consumption and sensing delay. Figure 4 and figure 6 show the schematic of VMSA and CTSA respectively. Table 1 and Table 2 show the comparison between both sense amplifiers. Graphical representation shown in figure 8 and figure 9 Read '1' and Read '0' operations have been performed on SRAM cell. For schematic design and simulation purpose Tanner EDA is used and technology used is 90nm.

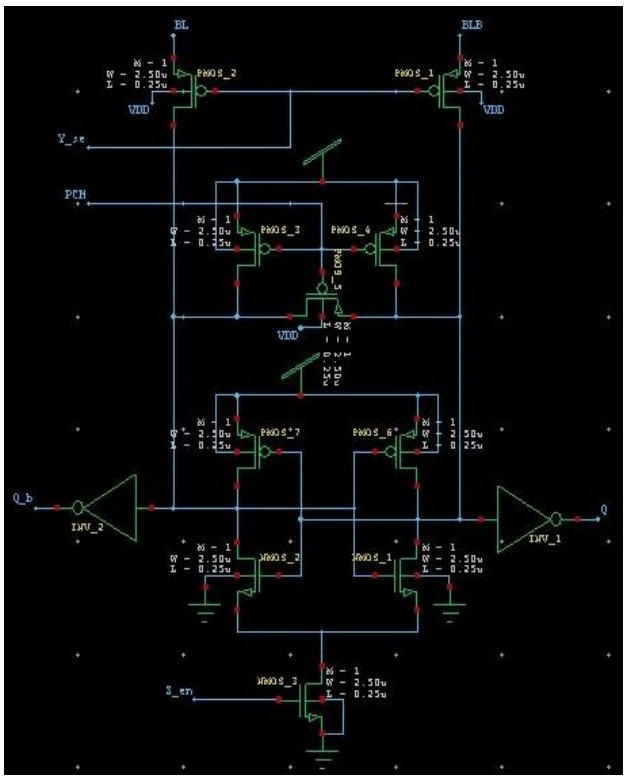

FIGURE 4: SCHEMATIC OF VMSA

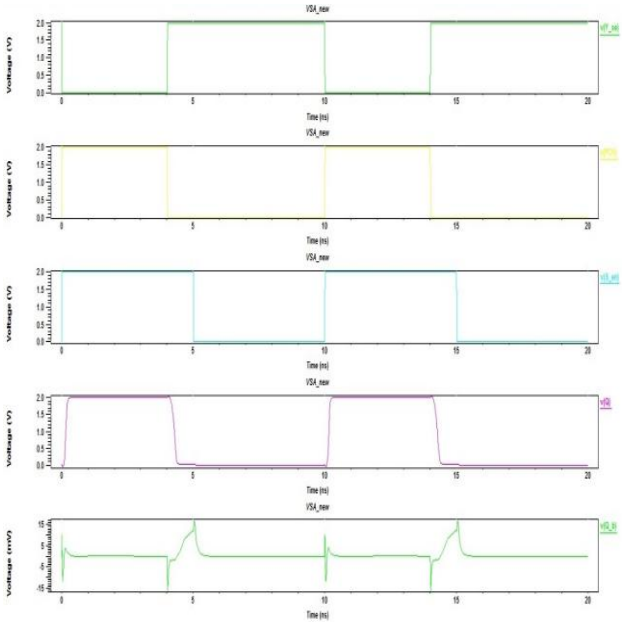

FIGURE 5: WAVEFORM OF VMSA

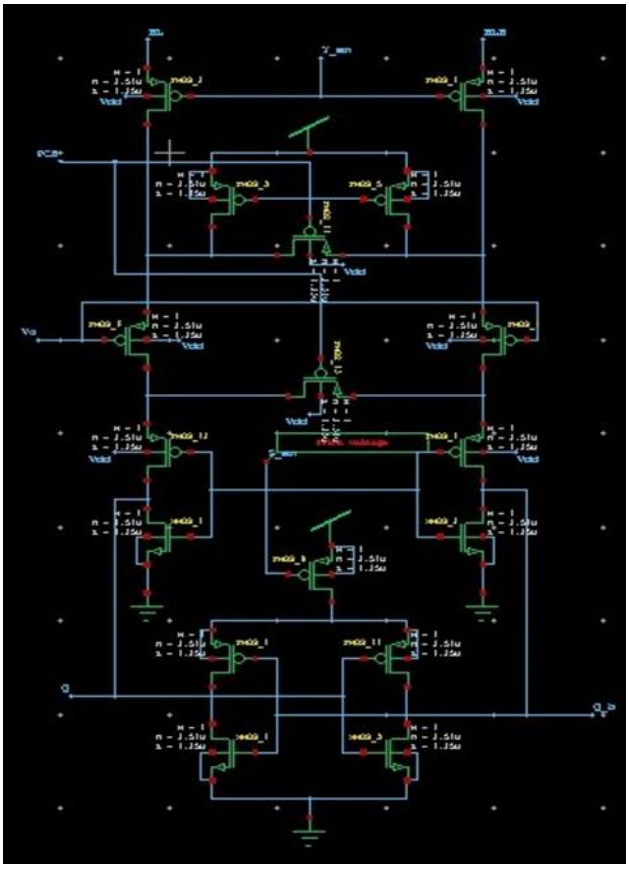

FIGURE 6: SCHEMATIC OF CTSA

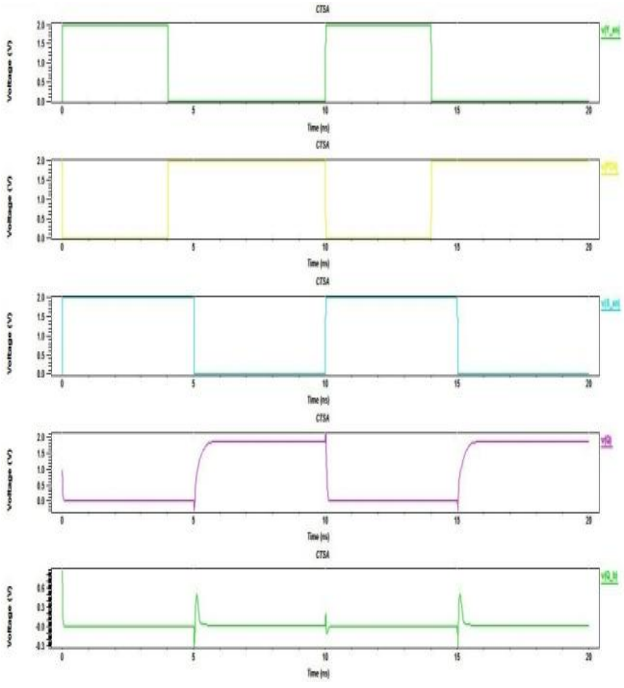

FIGURE 7: WAVEFORM OF CTSA

TABLE 1
COMPARISON OF AVERAGE POWER CONSUMPTION WITH VARYING SUPPLY VOLTAGE

S. No.	Voltage	Power Consumption(µW) at 90nm	
	(Vdd)	VMSA	CTSA
1	1.2V	17.48µW	2.48µW
2	1.5V	32.55µW	11.87µW
3	1.8V	54.36µW	33.39µW
4	2.1V	93.18µW	68.44µW
5	2.4V	220.81µW	150.16µW

2.1 Average Power consumption:

The power is calculated for these two topologies. Average power consumption for reading 0 & 1 operation is found to be same. Table 1 shows that CTSA consumes least average power in comparison to VMSA. The observation also shows that with increase in supply voltage, there is increase in average power consumption. Figure 8 shows the comparison of power supply of both sense amplifiers by graph.

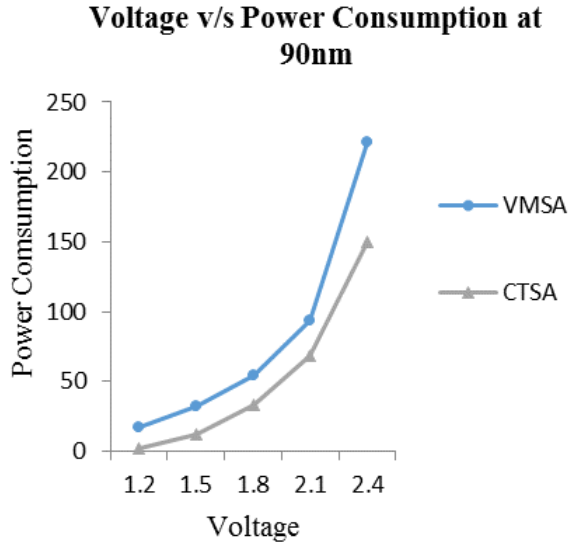

FIGURE 8: GRAPHICAL REPRESENTATION OF AVERAGE POWER CONSUMPTION

2.2 Sensing Delay

At 50% of logic levels Sensing Delay was calculated and it was observed that CTSA has the least delay in comparison to VMSA. Table 2 shows that with increase in supply voltage, delay decreases in both VMSA and CTSA. Figure 9 shows the comparison of sensing delay of both the sense amplifiers by graph.

TABLE 2
COMPARISON OF SENSING DELAY WITH VARYING VOLTAGE SUPPLY

S. No.	Voltage	Sensing Delay at 90nm	
	(Vdd)	VMSA	CTSA
1	1.2V	59.20 ps	70.73 ps
2	1.5V	48.20 ps	24.02 ps
3	1.8V	42.59 ps	19.33 ps
4	2.1V	38.59 ps	17.15 ps
5	2.4V	35.55 ps	15.72 ps

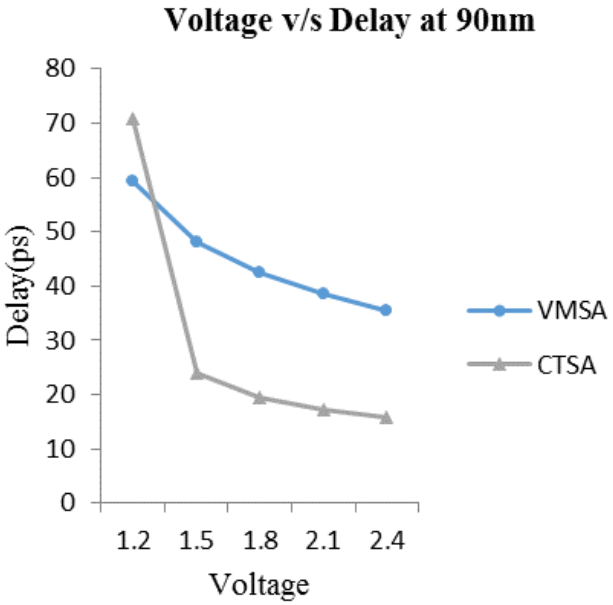

FIGURE 9: GRAPHICAL REPRESENTATION OF SENSING DELAY

III. CONCLUSION

In this paper SRAM with both the sense amplifiers i.e. Voltage Sense amplifier & Charge Transfer sense amplifier is analyzed and discussed. The observation shows that the CTSA give best results in terms of power consumption and sensing delay in comparison to VMSA. Observation of the work shows that power consumption of the sense amplifier is increases with the increase in supply voltage whereas sensing delay is decreases with increase in supply voltage. In future scope more efficient sense amplifier can be realized by improving available sense amplifiers so that power consumption and delay can be reduced during sensing the data from memory cell.

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