

# Design of RF Transmitter with high speed for Magnetic Resonance Imaging (MRI) using 8-Core DDS System of FPGA

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**Abstract**— An overall goal of the research is to investigate a new approach to the MRI RF Transmitter. Design a high-speed MRI RF transmitter. The goal is to explore the potential of a built-in DDS core of an FPGA chip to generate a dual-channel output at a 1 GHz sampling frequency of each. This output will be processed by a dual-input DAC chip for a total of 2 GHz sampling rate. The entire system should be able to generate the output signal ranging from 100 kHz to 750MHz. To accomplish this goal, it is necessary to study and to investigate the structures of these features to see how they could be utilized as a main core in a pulse generator

According to the datasheet provided by Xilinx, a DDS core has a single sine or/ and cosine output signal. The DDS core can operate at a maximum clock of 250 MHz. A 250 MHz clock speed is insufficient to generate outputs at 1 GHz sampling frequency. Consequently, the proposed custom DDS system is expected to quadruple the clock speed of the system by implementing multiple DDS core modules within the system.

**Keywords**— Direct Digital Synthesis.

## I. INTRODUCTION

### 1.1 Introduction of Magnetic Resonance Imaging

MRI spectroscopy is a technique used to study the physical, chemical and biological properties of materials by probing the nuclear dipole moments in the material. It was found and measured using molecular beams by Isidor Rabi in 1938. He received the Noble Prize in Physics in 1944 for his work. Two years later, Felix Bloch and Edward Mills Purcell expanded the technique to liquids and solids. They used it as an analytical tool in chemistry and physics in 1946.

An overall goal of the research is to investigate a new approach to the MRI RF Transmitter. The detail research objectives are as below:

**Design a high-speed MRI RF transmitter:** The goal is to explore the potential of a built-in DDS core of an FPGA chip to generate a dual-channel output at a 1 GHz sampling frequency of each. This output will be processed by a dual-input DAC chip for a total of 2 GHz sampling rate. The entire system should be able to generate the output signal ranging from 100 kHz to 750MHz. To accomplish this goal, it is necessary to study and to investigate the structures of these features to see how they could be utilized as a main core in a pulse generator. However, due to the limitations of FPGA to go beyond an allowable clock speed in DDS, the challenges of this problem lead to four objectives as below:

- Design a new topology for an MRI RF transmitter by using Matlab-Simulink. The Simulink is used to design the structures of a high-speed RF transmitter. The structures are verified through the Matlab-Simulink simulation.
- Simulate the designs in 1.3(a) above in the register-transfer level (RTL-level) simulation by using the Xilinx Verilog compiler. The simulations in Matlab do not consider the timing constraints within the DDS system. Matlab simulations are used to verify the functionality of the design and to analyze the flow from input to output. Therefore, it is necessary to simulate the design in RTL-level to ensure the behavioral structures meet the timing constraints.
- Design a new methodology to run a dual-output DDS module at 1 GHz each. The 1GHz frequency is beyond the clock limitation of an internal DDS core in an FPGA chip.

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## II. MATERIAL AND METHODS

### 2.1 Magnetic Resonance Imaging System

An MRI spectrometer requires a magnet, a coil, and some electronic systems such as a transceiver and a computer. These instruments provide the stimulus and to be subsequent detect the FID signal. First diagram figure 1 refers to the enlarged view of MRI system and figure2 refers to the block diagram of MRI Transmitter system.

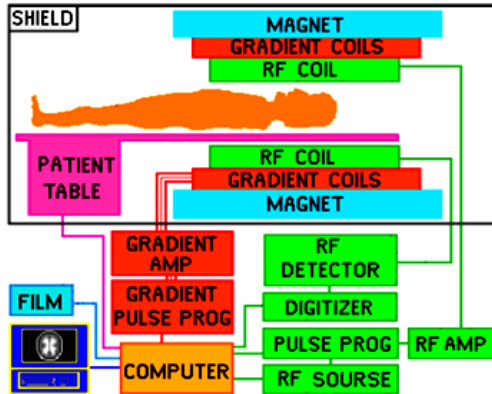


FIGURE 1: ENLARGED VIEW OF MRI SYSTEM

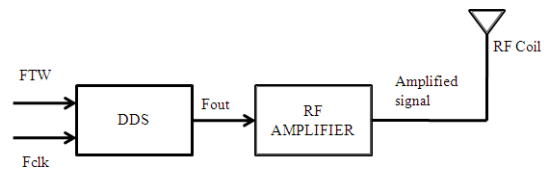


FIGURE2: BLOCK DIAGRAM OF MRI TRANSMITTER SYSTEM

Typically, the most expensive and difficult part of the system is the magnet system. The cost of the system is proportional to the magnetic strength. The better the sensitivity and spectral resolution of the system, and hence more expensive is the magnet.

The first block in Figure 1 refers to the DDS (Direct Digital Synthesis) block, which is used to generate the required output frequency upon providing the corresponding FTW (Frequency Tuning Word) and clock frequency. Thus the generated output frequency is fed to an RF Amplifier in order to amplify the signal to the desired level. Later the amplified signal is transmitted through RF Coil for further processing.

### 2.2 Direct Digital Synthesis

DDS usually refers to look-up table (LUT) based sinusoid generators. A DDS is a technique to generate frequency- and phase-tunable output signals.

It uses digital data processing blocks with a fixed-frequency precision clock to generate a sinusoidal signal. In Figure 2 a simple DDS can be created with a precision reference clock, an address counter, a Programmable Read-Only Memory (PROM) LUT and a DAC chip. In this basic system, PROM stores the amplitudes of a complete sine-wave. The address counter is used to generate memory addresses to access the PROM. A memory address is an identifier for a memory location in the PROM. The memory address will retrieve the digital amplitude from the PROM to the DAC chip. The advantage of using the DDS based system is that the simplistic architecture of the DDS system is less susceptible to the tuning flexibility. The reason is the output frequency can only be changed by modifying the system clock speed or by re-programming the step size in the PROM.

### 2.3 Phase Accumulator

The main part of the DDS system is the phase accumulator whose contents are updated once on each clock cycle. Each time the phase accumulator is triggered, the tuning word or phase increment,  $M$  is added to the contents of the phase accumulator. Let us assume that the initial content of the phase accumulator is  $00\dots00$  and  $M=00\dots01$ . The phase accumulator is updated by  $00\dots01$  on each clock cycle. A phase accumulator replaces the address counter in Figure 2 to introduce a function known as a 'phase wheel'.

Hence, a sine LUT is used to convert the output phases to sine-wave digital amplitudes. A DAC chip is then used to convert these amplitudes to an analog signal. However, the Nyquist sampling theory dictates a complete sine-wave must have at least two samples per cycle to construct the output waveform. Thus, the maximum frequency of an output sine wave is half of the DDS system clock.

In summary, the frequency of a sine-wave signal can be expressed by the equation below:

$$f_{out} = \frac{M}{2^N} f_{system} \quad (2.0)$$

$$M = \frac{f_{out} \times 2^N}{f_{system}} \quad (2.1)$$

$f_{out}$  = the frequency of an output sine wave signal

$M$  = frequency tuning word

$N$  = N-bit of a phase accumulator

$f_{system}$  = system frequency

'M' is also known as a digital number for phase hopping in an accumulation. 'N' is the total bits of a phase accumulator, so  $2^N$  is the amount of steps available in the accumulator.

The division of ' $f_{system}$ ' by  $2^N$  represents the frequency resolution of the system.

## 2.4 Phase-to-Amplitude Converter

In this thesis, the phase-to-amplitude converter or LUT is configured as a sine LUT. If B represents the width of a truncated phase, a sine LUT can be simply a read-only memory containing  $2^B$  samples that create the sample-domain waveform from the truncated phase received from the phase accumulator. In other words, it converts phases from a phase accumulator to amplitudes. These digital phases are also the memory addresses used to retrieve the corresponded amplitudes from the sine LUT.

A PROM can be used to implement a sine LUT. A PROM based LUT is easily implemented due to the simplicity of the PROM circuit. A LUT contains one complete cycle of the waveform to be generated.

The LUT translates the truncated phases into the sample amplitudes which are then converted to an analog signal by DAC.

If a high precision signal is required, the LUT needs a very large capacity as more bits are required to store the amplitudes. This increases the hardware cost and the implementation is limited by the capacity of the PROM. Practically, only the 'high bits' of an accumulated phase are used as a memory address to access the LUT. Generally, these high bits are known as the truncated phase. The size of a LUT is  $2^B$  words, therefore  $B < N$ ; N is the width of accumulated phases.

## 2.5 Taylor Series Corrected DDS

In the Taylor series corrected DDS; the previously discarded fractional bits have been used to calculate corrections to the phases. The corrections are added to the look-up table values to produce outputs with very high spurious free dynamic range (SFDR). This noise shaping technique can maintain the LUT to a reasonable size. The Taylor series corrected approximation is the expansion of a function of:

$$f(x) = f(a) + f'(a) \frac{(x-a)}{1!} + f''(a) \frac{(x-a)^2}{2!} + \dots \quad (2.1)$$

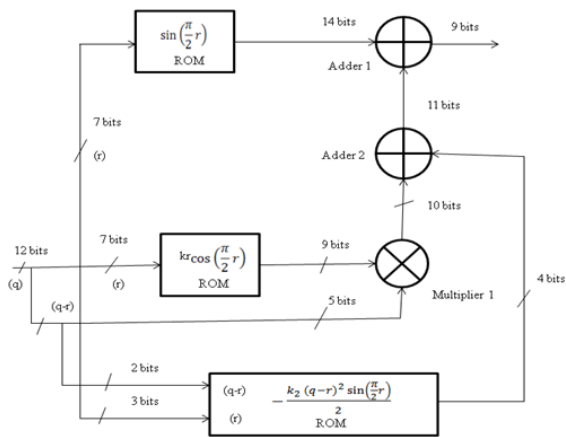
Hence, the Taylor expansion of  $\sin\left(\frac{\pi}{2} q\right)$  (quarter-wave storage in LUT) is as below:

$$\sin\left(\frac{\pi}{2} q\right) = \sin\left(\frac{\pi}{2} r\right) + k_1 (q - r) \cos\left(\frac{\pi}{2} r\right) - \frac{k_2 (q-r)^2 \sin\left(\frac{\pi}{2} r\right)}{2} + \dots \quad (2.2)$$

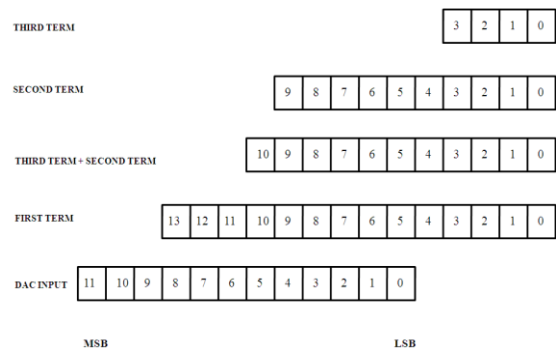
The total q-bit phase is divided into the upper phase 'r' and the lower phase 'q-r'. After the phase truncation, only the upper phase 'r' is used for the phase information, so the Taylor series is performed around 'r'.

The phase values have angular units so the constant  $k_n$  ( $n=1, 2, 3, \dots$ ) is used to adjust the units of each series term.  $k_n$  includes a multiple of  $\pi/2$  to compensate for the phase units.

It is also used to make sure the expression is always positive. From equation,  $k_1$  is  $\pi/2=1.57$  and  $k_2$  is  $-(\pi/2)^2 = -2.47$ . The Taylor series approximation takes up to three terms. In fact, additional terms can be employed but the contribution to the accuracy is very small. This architecture needs two read-only memory (ROM) blocks to store  $\sin(\pi r/2)$  and  $\cos(\pi r/2)$ . The unit conversion factor  $k_n$  is included in the values stored in the sine and cosine ROMs



**FIGURE 3A: TAYLOR’S SERIES APPROXIMATION FOR QUARTER SINE WAVE.**



**FIGURE 3B: RELATIVE BIT POSITION OF DATA WORD IMPLEMENTED**

For example, an input phase (q) has 12 bits as shown in Figure 3. The upper 7 bits of ‘q’ are used as the upper phase increment ‘r’. This ‘r’ is transferred to both sine ROM and cosine ROM at the same time. The upper 7 bits are the address signals and hence determine the number of entries in the ROMs. More bits in the upper phase address result in a larger LUT with decreased speed and greater cost.

The  $\sin(\pi/2)$  ROM is the first term of the Taylor series expansion. The output from the sine ROM will then sum the other terms from the expansion to re-construct the final phase (Adder 1).

The output of the  $\cos(\pi/2)$  is configured to incorporate the predetermined unit conversion value  $k_1$ . The cosine ROM is less significant than the amplitude term. Thus, the output can be at lower accuracy and so 9-bit output number is used. The lower 5 bits (q-r) are used to compute the other two terms used in the Taylor series expansion. The ‘q-r’ is multiplied with the output from cosine ROM to generate the second term (Multiplier 1). The second term has 10-bit output number.

The MSB of output from the ‘multiplier 1’ has a bit alignment with the DAC input Least Significant bit (LSB). Because of the alignment, the output number ranges from 1 LSB to 1/1024 LSB of the final 10-bit DAC input used. Not all the bits after the ‘multiplier 1’ are needed to maintain the accuracy of the system.

Therefore, the system truncates the multiplication product to 10 bits. In any case, truncation to 10 bits after ‘multiplier 1’ was used in the example in Figure 3. Any bit widths can be used as desired as long as the principles of the design are met. The third expansion term is computed in a ROM by combining the derivative of  $\sin(\pi/2)$  and  $(q-r)^2$ . This is done by selecting the upper 2 bits of ‘q-r’ and the lower 3 bits of ‘r’ as a portion of the address for the ROM. This is possible because the last expansion term only contributes roughly 1/4 LSB to the DAC input as shown in Figure 3B. In Figure 3, only the ‘r’ is needed for this degree of accuracy. Finally, the third term ROM output will combine with the ‘multiplier 1’ output in ‘Adder 2’. Subsequently, the result will combine with the first term ROM output in the ‘Adder1’.

### III. SIMULATION RESULTS

#### 3.1 Matlab-Simulink Simulation Results

15 MHz is randomly chosen as the frequency to test a single DDS core and few random frequency signals are used to test the 8 core DDS System. Finally a 64MHz frequency signal has been generated using 8 Core DDS System.

#### 3.2 Simulation Results of a Single DDS Core

The purpose of running the simulation on a standard DDS core is to observe the relationship between the phases and the amplitudes generated by the core. The explicit sample period of the phase accumulator and LUT is set to 8 in order to standardize the sampling period between a single DDS core and an 8-core DDS module. Consequently, the outputs of both simulations can be compared (both outputs have the same sampling period). The simulation is based on the Simulink design in Figure 4.1. The parameters of the simulation are:

- $F_{out}$  : 15000000 Hz
- Phase Accumulator System Clock,  $f_{system}$  : 250 MHz

Explicit Sample Period of Phase Accumulator core : 1  
 Simulation Period : 500 units

The simulation period is set to 500 units of time so that the design system can generate a couple of complete of sine-waves within this period. When the simulation is executed, 15000000Hz is converted to the frequency tuning word in the phase register block. The step-size of the output equals the phase increment of the output frequency. Based on equation (2.0), the tuning word is 2013265. Hence, the step size is 2013265. The frequency resolution is fixed at 7.45Hz for a Single DDS core with 250MHz system clock and 25-bit phase accumulator. The simulation results of Single DDS stage by using MATLAB are shown in Figure 4A and Figure 4B.

Tuning word= $15000000 \times 2^{25} / 250\text{MHz} = 2013265$

Step size= $2013265 / 1 = 2013265$

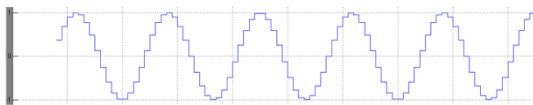


FIGURE 4A: 15MHz SINE WAVE (RF) SIGNAL (MATLAB)

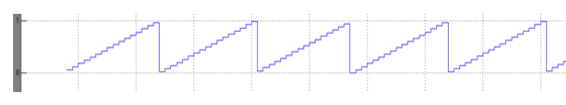


FIGURE 4B: PHASE OF 15MHz SINE WAVE (RF) SIGNAL (MATLAB)

The System Generator tool converts the design of Xilinx Blockset based Single DDS into Verilog HDL. In the design of Xilinx Blockset based Single DDS the inputs are ‘clock (250MHz)’, ‘rst’ and phase\_in’ which is 25-bit binary data. The output ‘sine’ is a 14-bit binary data and ‘phase’ is 25 bit binary data. The input ‘phase\_in’ is the phase accumulator input (holds the FTW). The outputs ‘sine’ is the digital amplitude sine wave signal and ‘phase’ is the phase of the signal. The simulation results of Single DDS stage by using Xilinx ISE tool is shown in Figure 5.

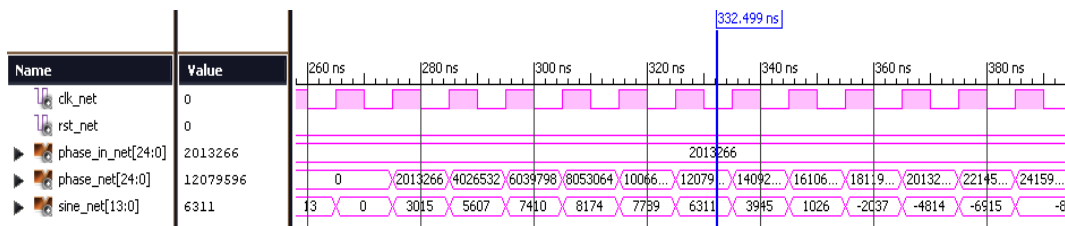


FIGURE 5: SIMULATION OF 15MHz SINE WAVE (RF) SIGNAL (XILINX)

With reference to the Figure Simulation of 15MHz sine wave (RF) signal (Xilinx), the phase\_in (FTW) for 15MHz signal is calculated based on equation (2.0) is given as input to the phase accumulator block in the DDS core. Upon pos-edge ‘clk’ and active low ‘rst’, the phase accumulator increments its value to FTW. Further these values are given as input to Sine LUT in DDS core, which performs phase to amplitude conversion.

The normalised tuning word on the phase register block is measured as 0.25 (Display\_tw). This 0.25 is divided by eight (denominator) to produce 0.03125 (normalised step size) via a divider block. 0.03125 is then multiplied by 2x D2, 3x D3, 4x D4, 5x D5, 6x D6, 7x D7 and 8x D8 to produce 2<sup>nd</sup> to 8<sup>th</sup> phase offsets. Each phase offset is combined with an accumulated phase from the ‘phase\_out’ through the respective Adder1 until Adder8. This methodology generated eight continuous samples ‘Out1’ to ‘Out8’ over a unit time. The results are shown in Table1.

TABLE 1  
 COMPARISON BETWEEN SIMULINK AND MATHEMATICAL CALCULATION RESULTS

Display	Simulink	Mathematical Calculation (Integer)
Display_tw	0.25	$0.25 \times 2^{25} \approx 8589934$
Display_Offset1	0.03125	$0.03125 \times 2^{25} \approx 1073741$
Display_Offset2	0.0625	$0.0625 \times 2^{25} \approx 2147482$
Display_Offset3	0.09375	$0.09375 \times 2^{25} \approx 3221223$
Display_Offset4	0.125	$0.125 \times 2^{25} \approx 4294964$
Display_Offset5	0.15625	$0.15625 \times 2^{25} \approx 5368705$
Display_Offset6	0.1875	$0.1875 \times 2^{25} \approx 6442446$
Display_Offset7	0.21875	$0.21875 \times 2^{25} \approx 7516187$
Display_Offset8	0.25	$0.25 \times 2^{25} \approx 8589934$

The results from the Simulink and mathematical calculations are identical. The normalised outputs can be restored to their original values by multiplying each normalised result with  $2^{25}$  (inverse of gain factor).

The System Generator tool converts the design of Xilinx Blockset based Phase Accumulator block into Verilog HDL. In the design of Xilinx Blockset based Phase Accumulator block, the inputs are ‘clock(250MHz),’ ‘rst’ and ‘tuningword’ which is 25-bit binary data and 8-sets of phase offsets as ‘offset1,offset2...offset8’. The outputs ‘phaseout1, phaseout2...phaseout8’ are 25-bit binary data. The input ‘tuning word’ is the phase accumulator input (holds the FTW) and ‘offset1, offset2...offset8’ holds the phase offset. The outputs are ‘phaseout1, phaseout2...phaseout8’ holds the 25-bit sample output phases.

The simulation results of Phase Accumulator block by using Xilinx ISE tool is shown in Figure6

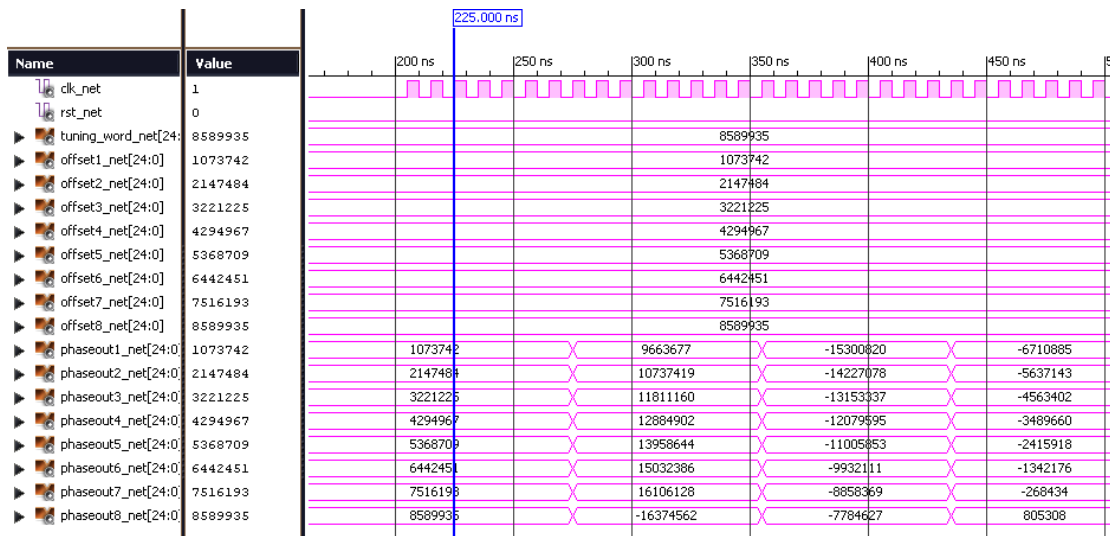


FIGURE 6: SIMULATION RESULTS OF 2 GHz PHASE ACCUMULATOR (XILINX)

### 3.3 Implementation results of Single DDS

The figure below shows the bus plot view of single DDS using chipscope.

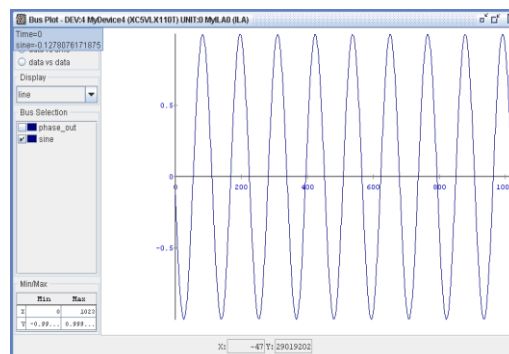


FIGURE 7: SINGLE DDS IMPLEMENTATION USING CHIPSCOPE

## IV. CONCLUSION

The RF Transmitter for Magnetic Resonance Imaging (MRI) is designed using 8-Core DDS System by Simulink Block set and Xilinx Block set. The System Generator tool converted the design into Verilog HDL. All these designs are simulated by using Xilinx ISE Simulator and then Synthesized by using Xilinx Synthesis Tool. All these designs are prototyped on Virtex-5 LX110T FPGA board. The RF Transmitter for Magnetic Resonance Imaging (MRI) is designed using 8-Core DDS System by Matlab Simulink Library and System Generator Tool. The design is simulated for functionality by using Xilinx ISE simulator tool.

The synthesized RF Transmitter for Magnetic Resonance Imaging (MRI) using 8-Core DDS System has 1099 LUT slices, 719 slice registers and 2 buffers. Timing analysis results show that the critical path is 3.091 ns i.e., the maximum clock frequency is 323.520MHz. The synthesized RF Transmitter for Magnetic Resonance Imaging (MRI) using 8-Core DDS System was successfully implemented on Xilinx Virtex 5 FPGA.

The RF Transmitter for Magnetic Resonance Imaging (MRI) can be extended to multi-frequency RF Generator. The design can cover the frequency range from 100 KHz to 750MHz.

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