Software based reconfiguration for the Cascaded H-Bridge multilevel converter

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Abstract— *Multilevel converters have been widely accepted in medium and high power applications, their general function is to synthesize a desired AC voltage from several levels of DC voltages. For more levels, the total harmonic distortion of the output voltage, decreases, has better waveform quality, low stresses on switching devices and better performance. This paper presents the reconfiguration based software for a cascaded H-bridge multilevel converter of five levels used as active shunt filter, to obtain seven levels. The transformation of the model in terms of the sum and the difference of the square of the capacitor voltages is crucial for our developments. The reconfiguration depends on the difference of the capacitor voltages, the imbalance between each H-bridge voltage and the commutation frequency.*

Keywords— adaptive law, active shunt filter, multilevel converter, pulse width modulation, total harmonic distortion, software based reconfiguration.

I. INTRODUCTION

The multilevel converters are a power electronic device that synthesizes an AC output voltage from several levels of DC voltages. They are available in wide power ratings that range from few VA to several MVA, finding application particularly on renewable energies [1]-[4]. Because distributed power sources are expected to become increasingly in the near future, the use of a multilevel converter to control the voltage output, frequency, phase angle [5], from renewable energy sources, will provide significant advantages due to it fast response and autonomous control [6]. Some advantages of multilevel technology includes, improved output waveform quality, better electromagnetic compatibility (EMC), low switching losses and capability of management high voltages [7].

There are three multilevel converter classic topologies: diode clamped, flying capacitor and series cascaded H-bridge (CHB). Diode clamped and flying capacitor needs more complex PWM controls, because more capacitors and diodes are needed for more output voltage levels. In the case of CHB each H-bridge has an independent DC source. Control and operation of this converter are simple and have robust structure than mentioned converters. The number of output levels is defined by $n = 2N + 1$, where N represents the number of DC sources which may be obtained from batteries, fuel cells or photovoltaic solar cells [8]-[9].

The asymmetric multilevel converters with unequal DC sources have been gaining attention, because they can synthesize output waveforms with a reduced harmonic content, even using a few series connected cells. The main objective is to obtain more output voltage levels without increase the power semiconductor devices or DC sources, reducing the total harmonic distortion that eliminates output filters [10]. Some authors combine different voltages, different topologies or even switch converters and linear amplifiers for hybrid asymmetric multilevel converters [11]-[13]. By properly designing and controlling the converter, it is possible to modulate the low voltage cells at inverter pulse width modulation frequency [14]. The power devices managing high voltage, switch at reduced frequency, decreasing switching losses [15].

Multilevel converters employ different modulation techniques for getting a better output voltage with the minimum harmonic distortion. The carrier based pulse width modulation, selective harmonic elimination, space vector modulation are some of the commonly use modulation for multilevel converters [16]-[17].

This paper presents the mathematical model and control process for the software reconfiguration of a CHB multilevel converter used as active shunt filter in order to obtain more output voltage levels [18]. The work is organized as follows. On section two, the system description, its mathematical model and model transform are studied. Section three develops the reconfiguration for obtaining seven levels output voltage. On section four, the results of the reconfiguration are exhibited. Finally, section five concludes the paper.

II. SYSTEM DESCRIPTION

The single phase CHB of five levels used as active shunt filter [19], as shown in Fig.1, is considered. The system dynamics can be obtained by Kirchhoff laws and transform it for design control purposes, yields the equations:

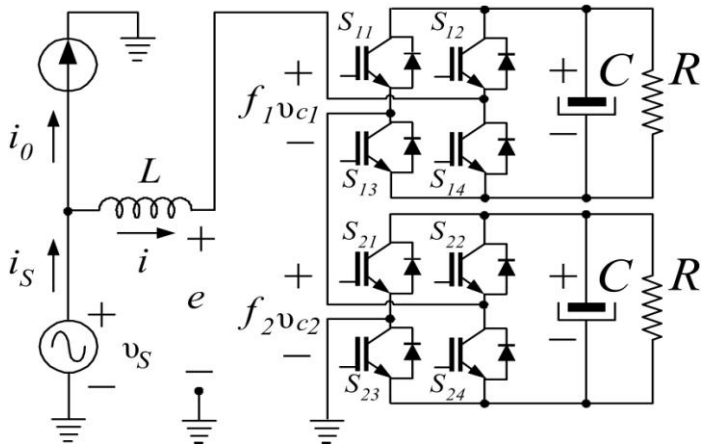

FIG. 1. CHB OF FIVE LEVELS.

$$L\frac{dx_1}{dt} = -L\frac{di_0}{dt} - \delta_1 + \upsilon_S \tag{1}$$

$$C\frac{dx_2}{dt} = \delta_1 x_1 - \frac{2}{R}x_2 \tag{2}$$

$$C\frac{dx_3}{dt} = \delta_2 x_1 - \frac{2}{R}x_3 \tag{3}$$

With the following definitions:

$$x_1 = i_S \tag{4}$$

$$x_2 = \frac{\upsilon C_1^2 + \upsilon C_2^2}{2} \tag{5}$$

$$x_3 = \frac{\upsilon C_1^2 - \upsilon C_2^2}{2} \tag{6}$$

$$\delta_1 = f_1 \upsilon C_1 + f_2 \upsilon C_2 \tag{7}$$

$$\delta_2 = f_1 \upsilon C_1 - f_2 \upsilon C_2 \tag{8}$$

The model is expressed in terms of the line current, the sum and the difference of the square of the capacitor voltages. The new variables δ_1 and δ_2 represents the actual control inputs. The complete system description can be found on [6].

III. RECONFIGURATION TO SEVEN LEVELS

The two H-Bridges depicted in Fig.1, have unequal DC-link voltage sources in the ratio 1:3. The H-Bridge in the higher voltage, commutates at lower frequency compared to the H-Bridge in the lower voltage, both bridges are switching following a sinusoidal pulse width modulation on phase disposition (SPWM-PD). Besides, for control design purposes the incoming assumptions were made:

- Decoupling assumption. It is surmised that, the inductor current dynamics is faster than the capacitor voltage dynamics. Then, the control is divided in two parts, an inner current loop, and the outer voltage loop.
- Odd harmonics. The load current i_0 and the line voltage v_S are periodic signals that contain odd harmonics of the fundamental frequency $\omega_0 = 2\pi f_0$, which is a known constant.
- Positive constants. The system parameters L, C and R are unknown positive constants.

Considering the assumptions stated above, the control design settle as follows.

3.1 Current tracking loop.

A control design δ_1 is designed to force the source current to follow a reference current signal proportional to the line voltage, that is:

$$x_1 = i_S \rightarrow i_S^* = \eta v_S \Big/ v_{S,RMS}^2 \tag{9}$$

Where $i_S^* = x_1^*$ represents the current reference, with $g = \eta \Big/ v_{S,RMS}^2$ a scalar representing the apparent conductance observed by the source. Thus equivalent to seek for an operation with power factor close to unity. Considering the error model of the current dynamics, can be obtained:

$$x_1^* = g v_S \tag{10}$$

$$L\dot{\tilde{x}}_1 = L\dot{x}_1 - L\dot{x}_1^* \tag{11}$$

$$L\dot{\tilde{x}}_1 = -\delta_1 + v_S + L\dot{i}_0 - L\dot{x}_1^* \tag{12}$$

$$L\dot{\tilde{x}}_1 = -\delta_1 + v_S + \sum_{k\in H} \rho_k^T \phi_k \tag{13}$$

Considering that:

$$\rho_k = \begin{bmatrix} \cos(k\omega_0 t) \\ sen(k\omega_0 t) \end{bmatrix}, \quad v_{S,k} = \begin{bmatrix} v_{S,k}^r \\ v_{S,k}^i \end{bmatrix}, \quad I_{0,k} = \begin{bmatrix} I_{0,k}^r \\ I_{0,k}^i \end{bmatrix} \tag{14}$$

Where numbers $I_{0,k}^r, I_{0,k}^i, v_{S,k}^r$ and $v_{S,k}^r \in \Re$ are the k^{th} harmonic coefficents of the Fourier series description of the load current and source voltage, respectively. The harmonic coefficients are assumed unknown and $H = \{1, 3, 5, \ldots\}$ is the set of indexes of the considered odd harmonics components.

The following controller is proposed:

$$\delta_1 = v_S + k_1 \tilde{x}_1 + \sum_{k\in H} \rho_k^T \hat{\phi}_k \tag{15}$$

This yields the following LTI system, referred as the error dynamics

$$L\dot{\tilde{x}}_1 = -k_1 \tilde{x}_1 - \sum_{k\in H} \rho_k^T \tilde{\phi}_k \tag{16}$$

Where $k_1 > 0$ is a design parameter and $\tilde{\phi}_k = \hat{\phi}_k - \phi_k$. The expression for δ_1 cancels v_S and adds a damping term $k_1(i_S - i_S^*)$ to reinforce stability. Following a Lyapunov approach as in [5], to obtain the complete expression for the controller, the next quadratic storage function is proposed:

$$V = \frac{L}{2}\tilde{x}_1^2 \sum_{k\in H} \frac{1}{2\gamma_k}\tilde{\phi}_k^2 \tag{17}$$

Where γ_k is a positive design parameter. Its time derivative along the trajectories of the error model is made negative semi-definite by proposing the adaptive law:

$$\dot{\tilde{\phi}}_k = \gamma_k \tilde{x}_1 \rho_k^T \tag{18}$$

This yields:

$$\dot{V} = -k_1 \tilde{x}_1^2 \tag{19}$$

The stability and convergence study of the proposed scheme can be completed using Barbalat's arguments [20], or using the signal properties [5].

Finally, following a similar approach as in [21], an expression for the harmonic compensation term $\hat{\phi}$ can be proposed. It consist on a bank of resonant filters, as describes below

$$\hat{\phi} = \sum \frac{s\gamma_l}{s^2 + l^2\omega_0^2}\tilde{x}_1 \tag{20}$$

Where γ_l with $l \in H$ is a positive design parameter. This harmonic compensator consist on a bank of harmonic oscillators tuned at the harmonics under concern, which confirms the well known internal model principle.

3.2 Regulation loop 1.

It is desire to drive the sum of the squares of the capacitor voltages towards a constant reference V_d^2, that is, $x_2 \to V_d^2$. This guarantees that enough energy has been stored in both capacitors for the correct fulfillment of the previous objective. Based on decoupling assumption, after a relatively short time $\tilde{x}_1 = 0$, and thus $\delta_1^* = v_S + L\dot{i}_0 - L\dot{x}_1$. Direct substitution of δ_1^* on (14) and taking the average value of the DC voltage zero component, neglecting the harmonic components, yields the following system:

$$\langle C\dot{x}_2\rangle_0 = g\langle v_S^2\rangle_0 - \langle v_S i_0\rangle_0 - \langle \frac{2}{R}x_2\rangle_0 \tag{21}$$

And using the definitions $\langle v_S^2\rangle_0 = \frac{1}{T}\int_{t-T}^{t} v_S^2\,dt = v_{S,RMS}^2$ and $\langle v_S i_o\rangle_0 = P_0$, the following system can be obtained:

$$\langle C\dot{x}_2\rangle_0 = g v_{S,RMS}^2 - P_0 - \langle \frac{2}{R}x_2\rangle_0 \tag{22}$$

Where P_0 is the DC component of the instantaneous output power. Notice that g is the actual control input. The proposed controller consist of a proportional plus integral (PI) terms, the proportional term is of limited bandwidth, both operating on the error signal $\tilde{x}_2 = (x_2 - V_d^2)$. This control is given below:

$$g = -k_{p2}\tilde{x}_2 - k_{i2}\int \tilde{x}_2 dt \tag{23}$$

3.3 Regulation loop 2.

Finally an expression for the control signal δ_2 is designed to drive the difference of the capacitor voltages to a constant reference α, that is $x_3 \to \alpha$. Based on decoupling assumption, it can be considered that, after a relatively small time $x_1 = X_1^*$, therefore the system (15) can be rewritten as:

$$C\dot{\tilde{x}}_3 = \delta_2 g v_S - \delta_2 i_0 - \frac{2}{R} x_3 \tag{24}$$

The control input can be proposed as $\delta_2 = v_S \chi$, direct substitution on (30) and taking the average value of the DC voltage zero component, yields the following system:

$$\langle C\dot{x}_3 \rangle_0 = g\langle v_S^2 \rangle_0 \chi - \langle v_S i_0 \rangle_0 \chi - \langle \frac{2}{R} X_3 \rangle_0 \tag{25}$$

Taking the definitions described on regulation loop, entails the system:

$$\langle C\dot{x}_3 \rangle_0 = g v_{S,RMS}^2 \chi - P_0 \chi - \langle \frac{2}{R} X_3 \rangle_0 \tag{26}$$

Notice that χ is the actual control input. The proposed controller consist of a proportional plus integral (PI) terms, both operating on the error signal $\tilde{x}_3 = (X_3 - \alpha)$. This control is given below:

$$\chi = -k_{p3}\tilde{x}_3 - k_{i3}\int \tilde{x}_3 dt \tag{27}$$

The full block diagram is shown in Fig. 2.

Summarizing, the changes proposed respect to CHB of five levels found in [6] to obtain the reconfiguration to CHB of seven levels are:

- The two H-Bridges has unequal DC-link voltage sources in the ratio 1:3.
- The two H-bridges use SPWM-PD, but commutates a different frequency. The H-Bridge in the higher voltage, commutates at lower frequency compared to the H-Bridge in the lower voltage.
- The current tracking loop and the balance loop remains intact, in the other hand, the regulation loop is driven to a reference constant α, instead to be zero.

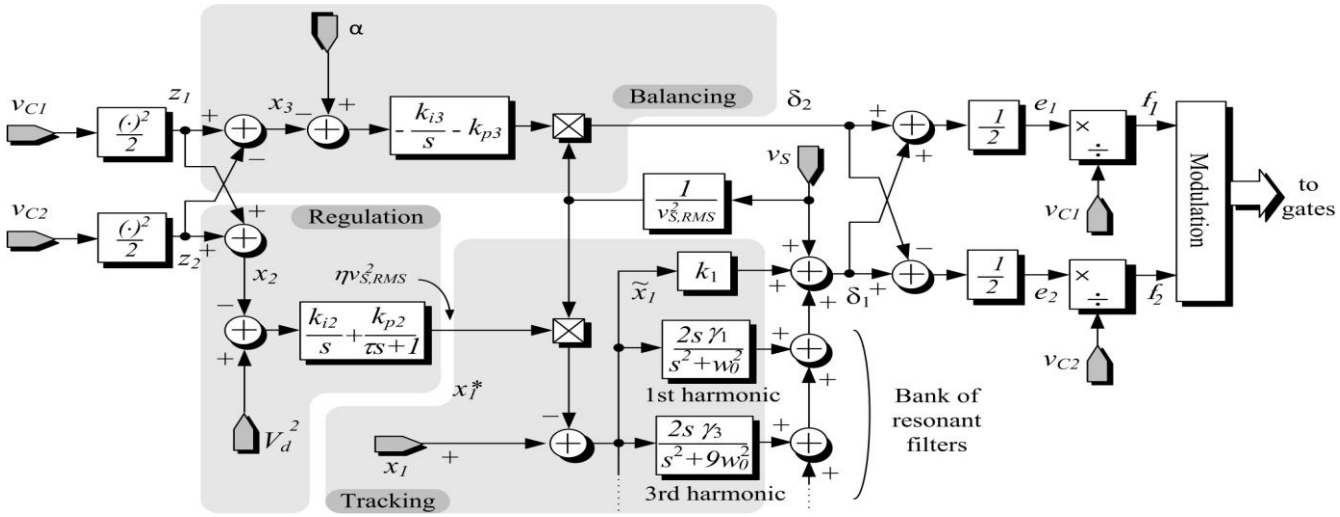

FIG. 2. BLOCK DIAGRAM OF THE OVERALL PROPOSED CONTROLLER.

IV. RECONFIGURATION RESULTS

In order to validate the reconfiguration, numerical results of the CHB of five levels using PSCAD 3.0 are developed. A voltage source of 127 V_{RMS} and $f_0 = 60\ Hz$ is considered. The voltage reference for the first bridge voltage was settled at 150 V and for the second bridge at 50 V, the commutation frequency was of 5 kHz and 15 kHz respectively. A diode bridge rectifier with a resistive load of $20\ \Omega$, and a bulky capacitor of 100 μF is regarded as nonlinear load. The active filter have been designed with the parameters L=3 mH, C=4400 μF and R=10 $k\Omega$.

In Fig. 3 from top to bottom, the regulation loop 1, regulation loop 2 and the CHB reconfigured output voltage are depicted.

Then in Fig 4, the THD of 10% of a CHB of five levels is shown.

Finally, the Fig. 5 shows the THD of 6% for the reconfiguration of a CHB of five levels to seven levels.

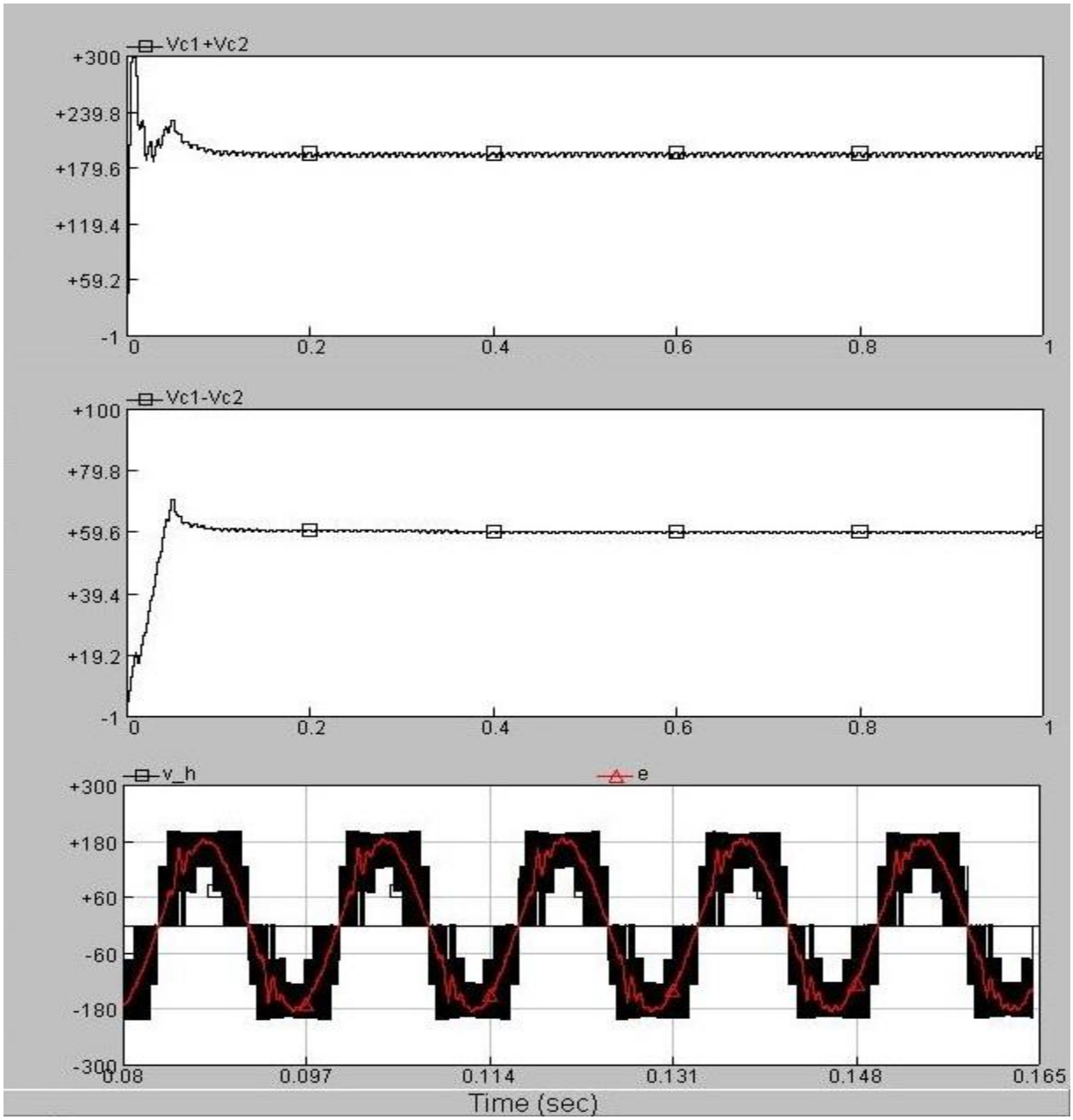

FIG. 3 RECONFIGURATION RESULTS.

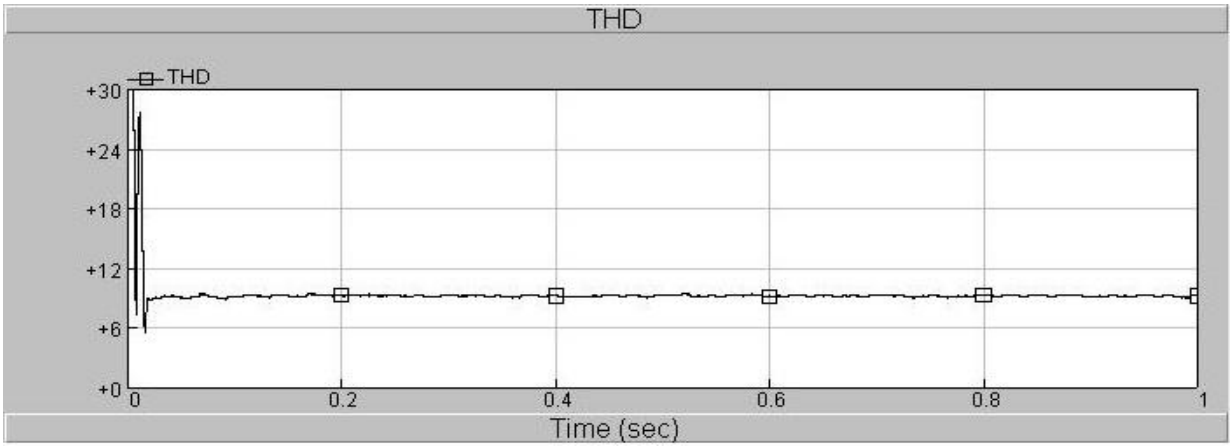

FIG 4. THD OF A CHB OF FIVE LEVELS OUTPUT VOLTAGE.

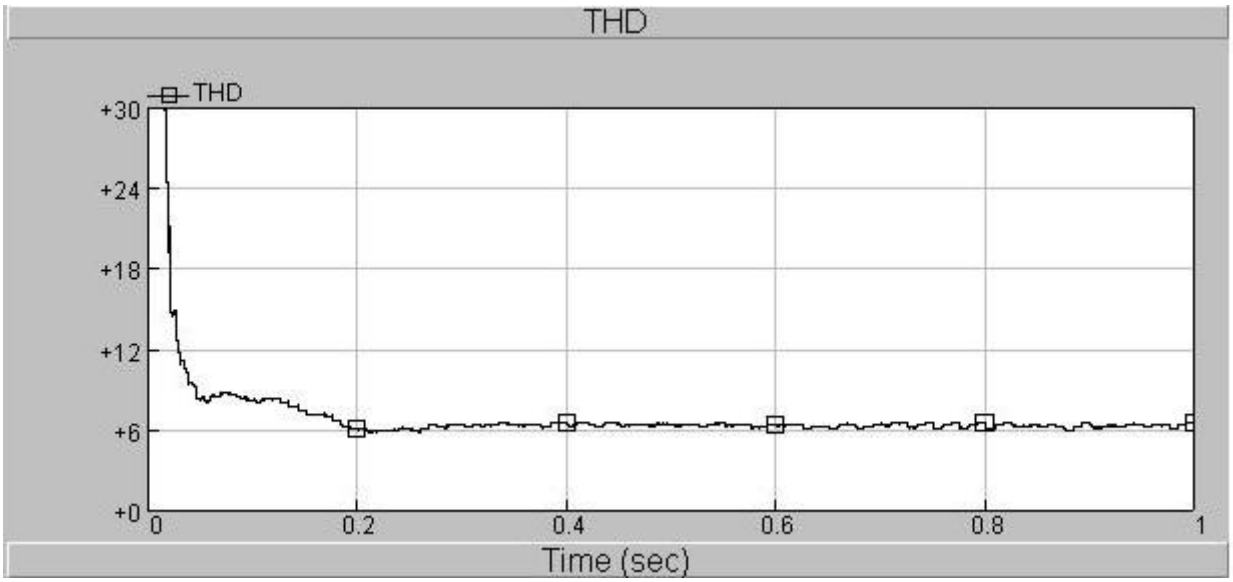

FIG. 5. THD OF A CHB OF FIVE LEVELS RECONFIGURED TO SEVEN LEVELS.

I. CONCLUSION

This paper presents the reconfiguration for the single phase CHB of five levels to obtain seven levels, used as active shunt filter. The reconfiguration was obtained through: modifying the capacitor voltage and the commutation frequency in the ratio 1:3, besides designing the two outer voltage loops to reach a desired voltage reference.

Numerical results using PSCAD have been included. It is remarkable the fact of the decrease of the THD until 6% on the reconfiguration output voltage against the 10% presented on a CHB of five levels output voltage, showing improvement of the results at more levels with the same hardware.

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