Power Improvement in 64-Bit Full Adder Using Embedded Technologies

Er. Arun Gandhi[1], Dr. Rahul Malhotra[2], Er. Kulbhushan Singla[3]

[1]Department of ECE, GTBKIET, Chhapianwali Malout, Punjab
[2]Director, Principal, GTBKIET, Chhapianwali Malout, Punjab
[3]Assistant Professor, GTBKIET, Chhapianwali Malout, Punjab

Abstract— *The adder is most commonly used arithmetic block of CPU (central processing unit) and DSP (digital signal processing), therefore its power and performance optimization is very important. With the scaling of technology to deep submicron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to increasing density of the chip. Therefore, in realizing modern VLSI circuits, low power and high speed are the two predominant factors which need to be considered. In this work, there is try to determine the best solution to this problem by improving the performance of adders.*

In this work, we improve and compare the power consumption of the three adders. The conventional full adder is built by 28 transistors. So, the transistor count is very high. The average power consumption and delay are very high. In this work, we consider three types of 64-Bit adders and try to improve their performance by varying width and length of substrate. For this purpose, we use tanner tool.

Keywords— CSL, CPL, DPL, Low power design.

I. INTRODUCTION

The adder is the most commonly used arithmetic block of the central processing unit and digital signal processing, Therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing modern very large scale integration (VLSI) circuits, low power and high speed are the two predominant factors which need to be considered. Like any other circuit's design, the design of high performance and low power adders can be addressed at different level, such as architecture, logic style, layout and the process technology. As a result, there always exists a trade-off between the design parameters such as speed, power, consumption and area.

Arithmetic circuits like adders are one of the basic components in the design of communication circuits. Recently, an overwhelming interest has been seen in the problems of designing digital systems for communication systems and digital signal processing with low power at no performance penalty. Designing low power, high speed arithmetic circuits requires a combination of techniques at four levels; algorithm, architecture, circuit and system levels. The remainder of this paper is organized as follows; section 2 describes the theoretical background. Section 3 describes the circuit designing and implementation of CSL, CPL and DPL adders. While corresponding experimental results and comparison of CSL, CPL and DPL adders are presented in section 4. Conclusion is described in section 5. Finally, future scope is given in section 6.

II. THEORETICAL BACKGROUND

The research efforts of the past years in the field of digital electronics have been directed towards the low power of digital systems. Recently, the requirement of probability and the moderate improvement in battery performance indicate power dissipation is one of the most critical design parameters. Day by day the demand of probability and mobility is increasing. Also the area of chip design is taken into consideration while talking about probability. Hence three most widely accepted parameters to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation.

The reduction of the power dissipation and the improvement of the speed require optimization at all levels of the design procedure. Since most digital circuitry is composed of simple AND/OR complex gates, The best way is to implement logic and arithmetic functions in order to achieve low power dissipation and high speed. Several circuit design techniques are compressed in order to find their efficiency in terms of speed and power dissipation. In these days, transistors are vused for designing logic gates, same transistors are used to design other blocks such as flip-flops or memories. Ideally, a transistor

behaves like a switch. For NMOS transistors, if the input is a 1 the switch is ON, otherwise it is OFF. On the other hand, for PMOS, if input is 0 the transistor is ON, Otherwise the transistor is off [2].

There are three major sources of power consumption in digital CMOS circuits, which are summarized in the following equation [1].

$$P_{total} = P_{switching} + P_{short-circuit} + P_{leakage}$$

$$= (\alpha_{0\to1} \times C \times V_{dd^2} \times f_{clk}) + (I_{sc} \times V_{dd}) + (I_{leakage} \times V_{dd}) \quad \textbf{(1)}$$

The first term represents the switching component of power, where C is the load capacitance, f_{clk} is the clock frequency and $\alpha_{0\to1}$ is the node transition activity factor. The second term is due to the direct path short circuit current, I_{sc} , which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, $I_{leakage}$, which can arise from substrate injection and substrate threshold effects, is primarily determined by fabrication technology considerations. However, while supply voltage reduction is the most effective way to reduce the power consumption, such a reduction require new design methods for low-voltage and low power integrated circuits. Since an average of 15-20% of the total power is dissipated in glitching, low power can also be achieved by reducing the glitches of the circuit [1].

III. CIRCUIT DESIGN AND IMPLEMENTATION

This section contains the circuit designing and implementation of CSL, CPL and DPL adders.

3.1 Conventional Static CMOS Logic (CSL)

Conventional static CMOS logic is used in most chip designs in VLSI applications. It consists of complementary NMOS pull-down and PMOS pull-up networks to drive '0' and '1' outputs. The features of this logic style are **;**

1. good noise margin
2. fast speed
3. low power
4. easy to design
5. robustness against voltage scaling
6. arbitrary transistor sizes

The schematic diagram of a conventional static CMOS AND gate and full adder cell is illustrated in figure 1 and figure 2 respectively [3].

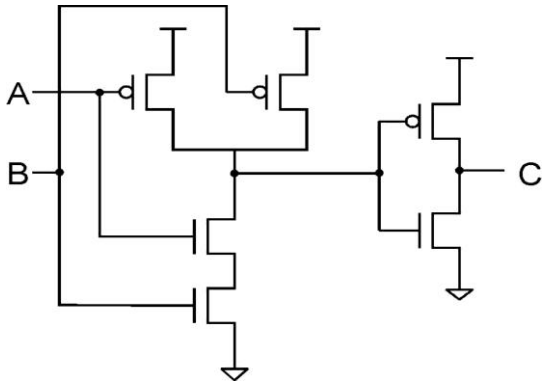


FIG.1 SCHEMATIC DIAGRAM OF CSL AND GATE

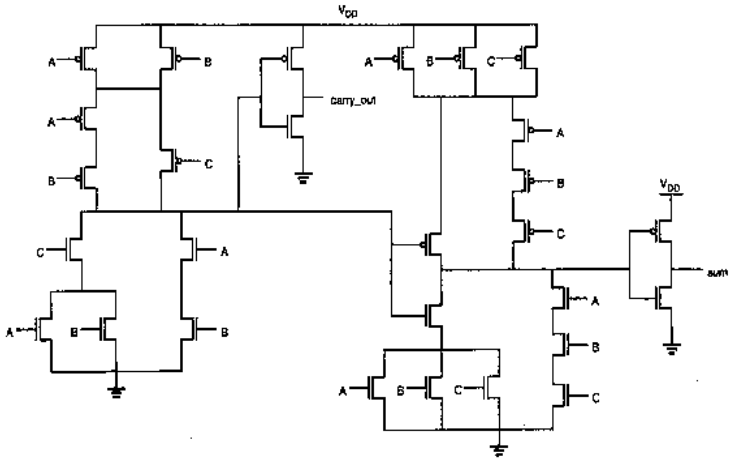


FIG. 2 SCHEMATIC DIAGRAM OF CSL FULL ADDER

3.2 Complementary PASS TRANSISTOR (CPL)

CPL consists of complementary inputs, outputs, an NMOS pass transistor logic network, and CMOS output inverters as shown in figure 3.

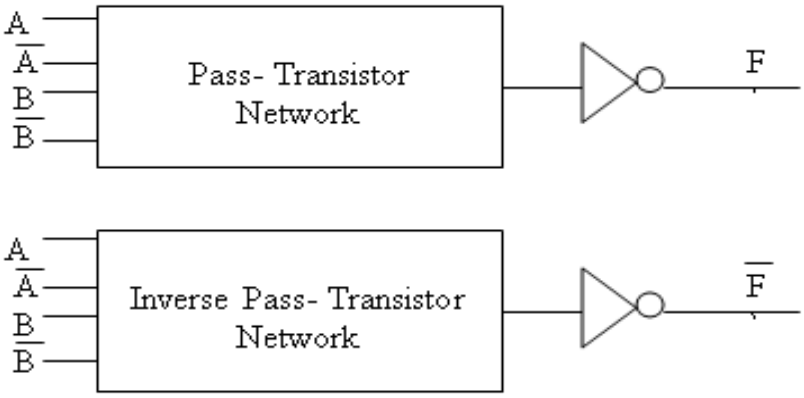


FIG.3 BASIC CONCEPT OF CPL

As inverted and non-inverted inputs are needed to drive the gates of the pass transistors, the complement of the logic also needs to exist. The pass-transistor network and inverse pass-transistor network is generate F and $\bar{F}$. The schematic diagram of the CPL AND gate and full adder circuit is shown in figure 3. The equations for figure 3 are given as [4]:

$$F = A.B + B.B = A.B \tag{2}$$

$$\bar{F} = \bar{A}.B + \bar{B}.\bar{B} = \bar{A}.B + \bar{B} = \bar{A} + \bar{B} = \overline{AB} \tag{3}$$

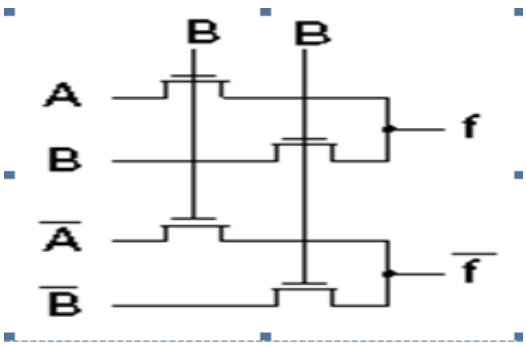


FIG. 4 SCHEMATIC DIAGRAM OF CPL AND GATE

3.3 Double Pass Transistor Logic (Dpl)

The DPL is a modified version of CPL. The DPL also has complementary inputs and outputs and thus it is implemented using dual-rails. In DPL circuits, full voltage swing is achieved at outputs by adding a PMOS transistor in parallel with NMOS transistors. Although the addition of PMOS transistors results in increased capacitance compared to CPL style but this does not limit the performance of DPL because DPL gates have balanced input capacitance, thus reducing the dependence of delay on input data.

The problems of noise margin and speed degradation in CPL circuits due to high reduced voltage level are solved out in DPL design style. The output buffers are not necessary, since the full swing is achieved by the addition of PMOS transistor. The schematic diagram of the DPL AND gate & full adder circuit is shown in figure 5 [5].

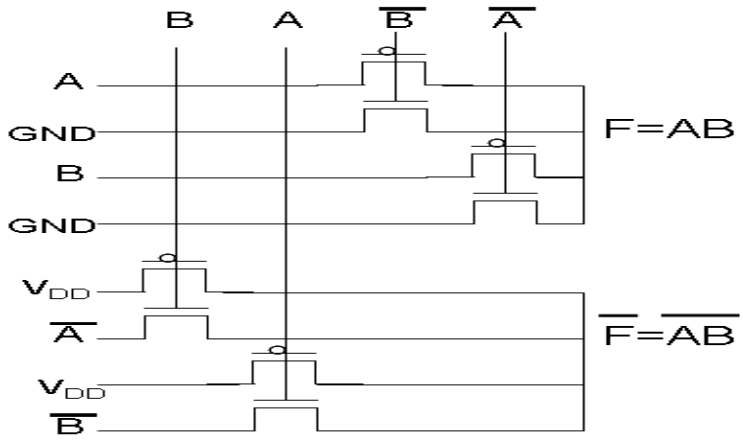
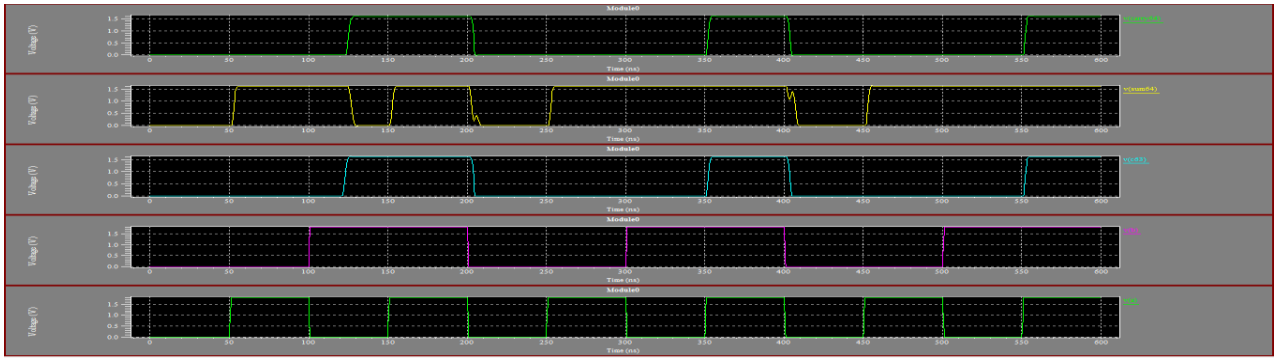


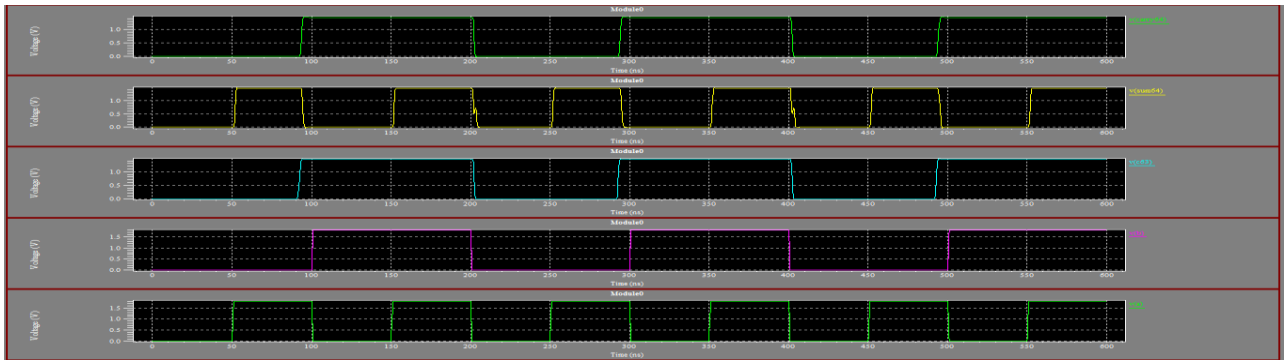
FIG. 5 SCHEMATIC DIAGRAM OF DPL AND GATE

IV. RESULTS & COMPARISON

4.1 Waveforms of CSL Full Adder

The waveforms of CSL adders using 90nm, 130nm & 180nm technologies are shown below in figure 6,





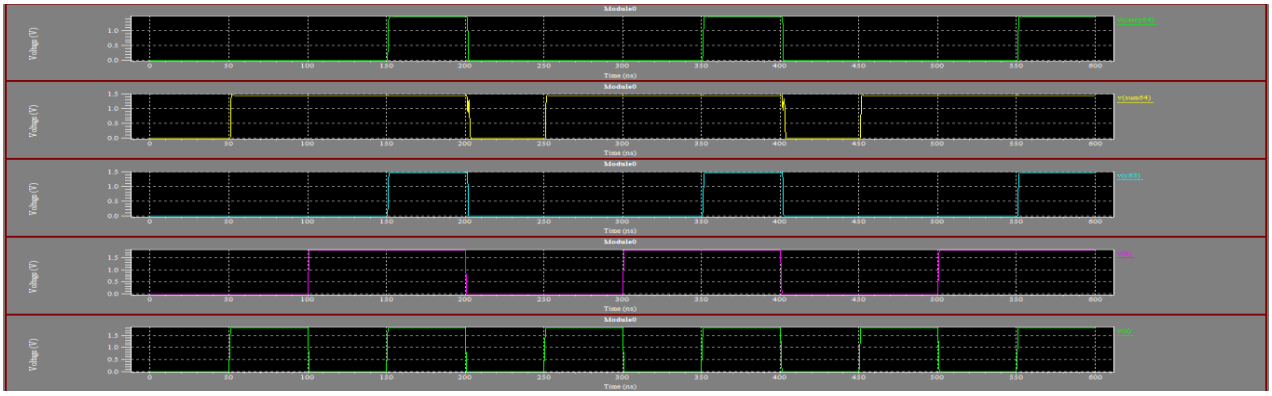


FIG.6 WAVEFORMS OF 64-BIT 90NM, 130NM AND 180NM CSL BASED ADDER

4.2 Waveforms of CPL Full Adder

The waveform of CPL full adder using 90nm, 130nm & 180nm technologies are shown below in figure 7. In this there are three inputs A, B and C & two outputs sum and carry.

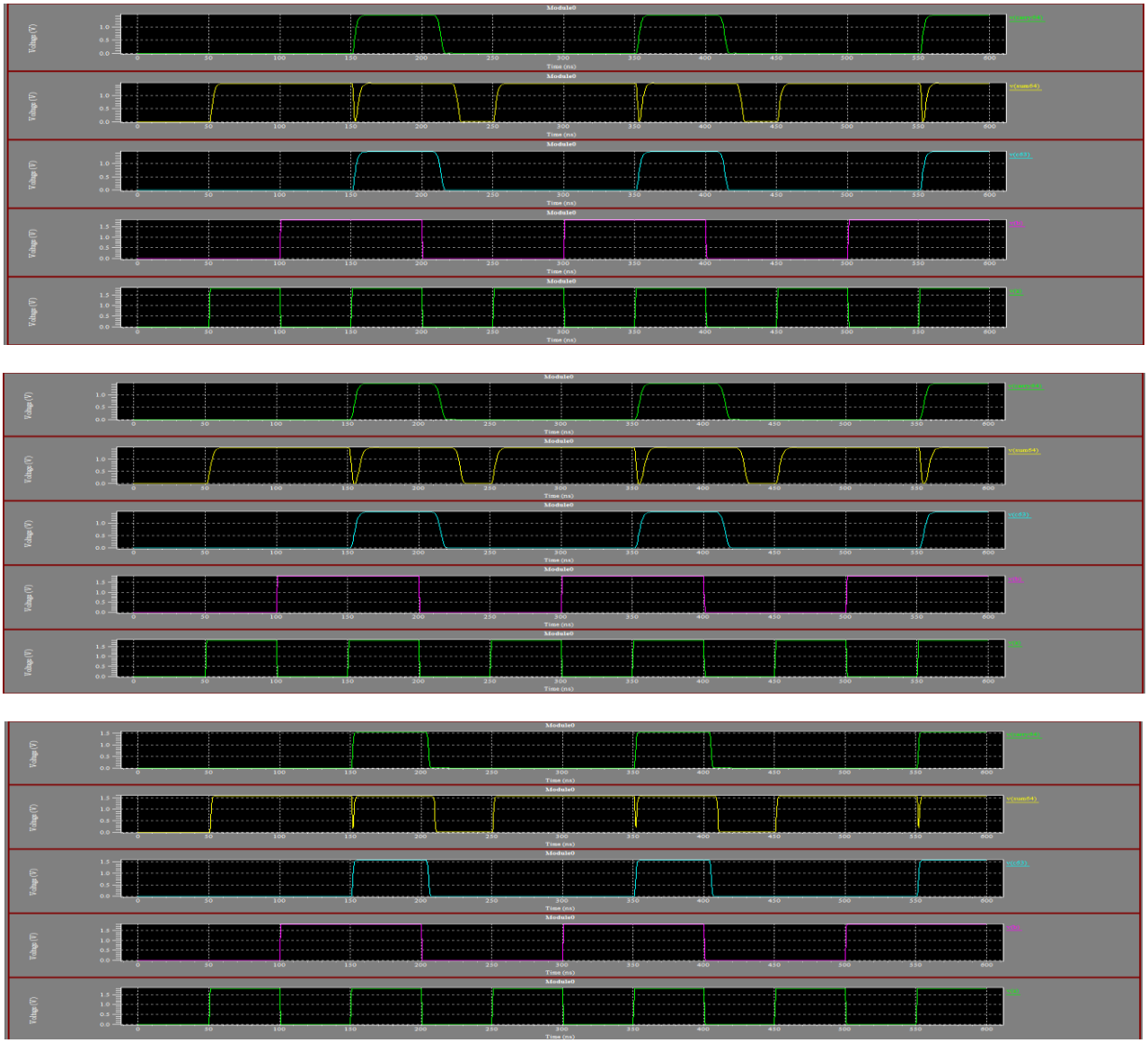


FIG. 7 WAVEFORMS OF 64-BIT 90NM, 130NM AND 180NM CPL BASED ADDER

4.3 Waveforms Of DPL Full Adder

The waveforms of DPL full adder using 90nm, 130nm & 180nm technologies are shown in figure 8. In this there are three inputs A, B, C and two outputs sum & carry

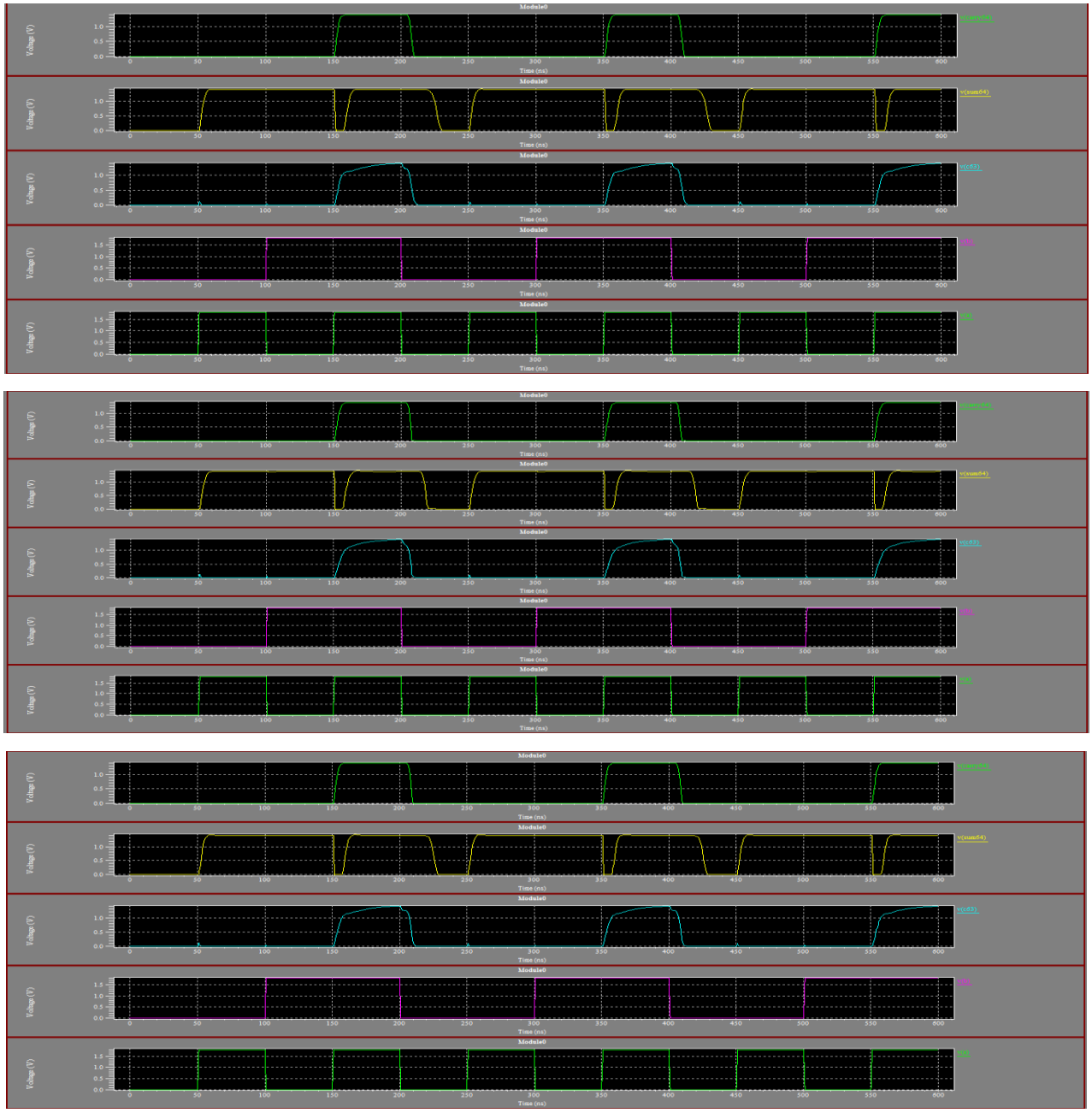


FIG. 8 WAVEFORMS OF 64-BIT 90nm, 130nm AND 180nm DPL BASED ADDER

In this design process, all simulations are done using 90nm, 130nm and 180nm technology process models with typical n-channel and p-channel drive, 0.9v,1.3v and 1.8v power supply. In the schematics, all logics are designed using a minimum gate length of 90nm, 130nm, 180nm and a minimum width of 135nm, 195nm, 270nm for NMOS and for PMOS 405nm, 585nm & 810nm gate width. According to the power dissipation, area and delay, CSL adder is better as compared to CPL and DPL adder.

TABLE 1
PERFORMANCE PARAMETERS OF 64-BIT ADDERS

Design Style	No. of transistors	Minimum Length (nm)	Width of NMOS(nm)	Width of PMOS (nm)	Avg. Power Consm. (watts)	Prop. Delay at Sum (sec)	Prop. Delay at carry(sec)	PDP at sum	PDP at carry
CPL	1408	90nm	135nm	405m	13.13485e-004	1.0102e-009	3.0941e-009	13.2688e-013	40.6405e-013
		130nm	195nm	585nm	17.21844e-004	1.2821e-009	3.5621e-009	22.0757e-013	61.3338e-013
	1792	180nm	270nm	810nm	13.99889e-004	0.65826e-009	1.0519e-009	9.2140e-013	14.7254e-013
		90nm	135nm	405nm	9.021230e-004	1.7360e-009	1.1399e-009	15.6608e-013	10.2833e-013
CSL		130nm	195nm	585nm	11.23279e-004	1.0321e-009	0.68040e-009	11.5933e-013	7.6427e-013
		180nm	270nm	810nm	6.801469e-004	1.8405e-009	0.372944e-009	12.5181e-013	2.5365e-013
DPL	2176	90nm	135nm	405nm	17.86772e-004	0.61063e-009	2.2289e-009	10.9105e-013	39.8253e-013
		130nm	195nm	585nm	22.74659e-004	0.29480e-009	1.7516e-009	6.7056e-013	39.8429e-013
		180nm	270nm	810nm	15.74452e-004	0.37272e-009	1.9032e-009	5.8682e-013	29.9649e-013

TABLE 2
COMPARISON OF PDP IMPROVED 64-BIT RESULTS VS PDP BASE PAPER 32-BIT RESULTS OF CSL, CPL & DPL BASED ADDERS

	PDP at sum (32-BIT base paper)	PDP at sum (64-BIT Enhanced)	PDP at carry (32-BIT base paper)	PDP at carry (64-BIT Enhanced)
CPL 90nm	7.2864e-013	13.2688e-013	25.1407e-013	40.6405e-013
CPL 130nm	15.6662e-013	22.0757e-013	49.5669e-013	61.3338e-013
CPL 180nm	4.1258e-013	9.2140e-013	7.5480e-013	14.7254e-013
CSL 90nm	27.7835e-013	15.6608e-013	5.3777e-013	10.2833e-013
CSL 130nm	6.6201e-013	11.5933e-013	4.9514e-013	7.6427e-013
CSL 180nm	6.4306e-013	12.5181e-013	1.3017e-013	2.5365e-013
DPL 90nm	6.1845e-013	10.9105e-013	18.5423e-013	39.8253e-013
DPL 130nm	4.0853e-013	6.7056e-013	21.5572e-013	39.8429e-013
DPL 180nm	3.6044e-013	5.8682e-013	13.2098e-013	29.9649e-013

V. CONCLUSION

Focus of this paper was mainly on high performance and low power adder. The adder designed in this work provides the low power requirement. It also presents an area efficient approach to low power, less number of transistors for any design.

64-bit adders were designed in tanner (Evaluation version) tool using 90nm, 130nm and 180nm and analysis of dynamic power dissipation, delay and area was done. Table 1 above shows the power and delay comparison among CSL, CPL & DPL adders. The table 2 above shows comparison between enhanced 64-bit PDP results and base paper 32-bit PDP results.

VI. FUTURE SCOPE

CSL, CPL, DPL based advanced full adder circuit reduces the transistor count, power consumption and delay of the circuit. The work of this paper may be further extended by various ways as :

- The work can be extended to 128-bit adders.
- The research steps may be taken further to optimize the parameters like using frequency, capacitance, length, width etc.
- The work can be extended to change the technology file.
- The efforts can be made to decrease the transistor count further power, area and delay can be minimized by changing the parameters.
- Research steps can be taken by using the other types of adders like ripple carry adder, hybrid adder etc

REFERENCES

[1] A. Morgenshteinet.all, "Gate Diffusion Input (GDI): A Power Efficient Method for Digital Combinatorial Circuits", IEEE transactions on VLSI systems, vol. 10, pp. 566-581, 2002.

[2] A. P. Chandrakasanand W. Brodersen, "Minimizing Power Consumption in Digital CMOS Circuits", Proceedings of the IEEE, vol. 83, no. 4, pp. 498-523, 1995.

[3] K. Roy et.all, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits", Proceedings of the IEEE, vol. 91, no. 2, pp. 305-327, 2003.

[4] S. Mukhopadhyayet.all, "Gate Leakage Reduction for Scaled Devices Using Transistor Stacking", IEEE transactions on very large scale integration (VLSI) systems, vol. 11, no. 4, pp. 732-730, 2003.

[5] I. S. Abu-Khateret.all, "Circuits Techniques for CMOS Low-Power High Performance Multipliers", IEEEJournal of Solid-State Circuits, vol. 31, no.10, pp. 1535-1546, 1996.

[6] A. Fish and I. Shwartz, "Gate Diffusion Input (GDI) Logic Standard CMOS Nanoscale Process", 26th convention of IEEE in Israel, pp. 776-780, 2010.

[7] D. Wang et.all, "Novel Low Power Full Adder Cells in 180nm CMOS Technology", Industrial Electronics and Applications, 4th IEEE Conference on Digital Object Identifier, pp. 430-433, 2009.

[8] P. G. Parateet.all, "ASIC Implementation of 4 Bit Multipliers", First International Conference on Emerging Trends in Engineering and Technology, IEEE, pp. 408-413, 2009.