Power Efficient Digital LDO Regulator with Transient Response Boost Technique

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Abstract— *A digital low-dropout regulator (D-LDO) with reduced transient response time and overshoot/undershoot is proposed. The reduction of response time is achieved by using transient response boost technique. The loop gain is increased at the time of deviations exceeding the limit and the loop gain is returned after the output voltage is settled. On comparing LDO with and without transient response boost technique the settling time is reduced. The regulation is done in time mode with the help of high linear voltage to time convertor (VTC) and time to digital convertor. The time domain analog to digital conversion achieves high resolution at low power and small area. And multibit cyclic TDC for high level current efficiency is used.*

Key words—Current efficiency, cyclic TDC, digital low-dropout regulator (D-LDO), transient-response boost mode (TRBM), voltage-to-time converter (VTC).

I. INTRODUCTION

Nowadays the battery powered devices are increased and various applications are embedded in a single device as seen in various SoCs. Here the power management unit plays an important role since the power from battery is limited in capacity. The on-chip LDO are gaining more attention as a power management unit. However, most of research works on the low-dropout voltage regulator still focus on the analog control. Compared to the design flow of the analog approach, the digital design flow presents the following difference: designers specify the size of power MOSFET, load requirement, output capacitor value, and its ESR value. In case of analog LDOs driving near threshold and sub-threshold logic circuits a difficulty is imposed in maintaining the low dropout voltage. The time domain ADC can provide higher resolution.

The simple structure of LDO composed of simple convertor consisting binary comparator and shift register. The transient response time is reduced by means of increasing the clock frequency [5] which can be achieved with the help of asynchronous shift register. Multibit ADC provide faster loop operation through direct measurement of voltage difference.TDC based 4-bit ADC with Proportional-Integral-Derivative(PID) controller provide stability compensation and fast transient response is achieved through dynamic clock scaling but it results in high quiescent current. The ADC without PID controller results in higher voltage ripples due to insufficient resolution. Thus power efficient digital linear LDO regulator based on multibit cyclic TDC for high level current efficiency is employed.

II. RELATED WORK

A digitally controlled low-dropout voltage regulator with fast transient response and auto-tuned voltage is achieved by means of an autotuning algorithm [3]. Test of the autotuning algorithm shows that the LDO is able to work at its optimal performance under various uncertain conditions and even when the supply voltage is going lower. Digital controller processes discrete signal and operate with logic gates. No matter what the scale of the supply voltage is, so long as the supply voltage ensures the normal operation of logic gates, there is no impact of the voltage level on the compensation design. Accordingly, the transfer function is derived for choosing appropriate type of the compensator. This design flow also allows designers to implement programmable features which are more suitable for customization. In charge balance algorithm [3], from frequency analysis point of view, the cross-over frequency is limited by the phase margin to ensure enough stability margins. However, confining the cross-over frequency to some range may slow down the transient response of the power converter. To speed up the transient response without increasing the cross-over frequency [5], a charge balance concept is used and it was successfully applied to dc–dc switching converter. Due to the different operation principles between the switching converter and the LDO regulator, the charge balance algorithm should be revised before applying to the LDO. Additionally using the asynchronous shift register, instead of the typical synchronous shift registers is efficient. But, it still has a problem, in that circuit operation is too sensitive to PVT variation, to get constant performance between chips. A

multibit ADC can provide faster loop operation through direct measurement of the voltage difference. Also, it allows for designers to implement the algorithms of more complex loop compensation and loop acceleration.

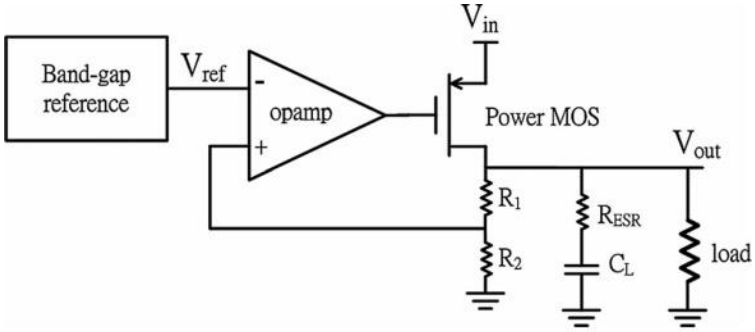

FIGURE 1 SIMPLE STRUCTURE OF LDO

Digital LDO with PLL

A Conventional D-LDO regulator adopting the synchronous control scheme in which the operation is realized using clock signal. The comparator is used to compare the output voltage with the reference voltage and the power switches are activated using the shift registers. When large output power is requested to the D-LDO regulator, the comparator would detect the occurrence of insufficient energy at the so that more power switches are turned on to provide the supplementary current. Operating clock frequency is the main parameter affecting the performance of the synchronous D-LDO regulator. Due to the infinite bandwidth of the comparator, the shift register can be immediately informed to either increase or decrease the driving capability of power switches when the output loading is changed. Shift registers determined the transient speed because the shift register allows only one power switch to be turned on or off within per clock cycle in the synchronous D-LDO regulator. If the synchronous D-LDO regulator operates with a slow frequency clock, small power consumption realizes the better current efficiency, compared with current efficiency which is derived with the fast frequency clock [4]. This result in larger current dissipation and due to the usage of slow clock frequency speed is affected. However, fast tracking speed can be achieved by adopting the high frequency clock in a synchronous D-LDO regulator but results in the worse current efficiency compared with that when operating with a slow frequency clock . That is, higher frequency operation leads to faster voltage tracking speed. Moreover, the current efficiency of the D-LDO regulator is inversely proportional to the frequency of the clock signal. Fast voltage tracking speed can be ensured; however, current efficiency will be deteriorated in the synchronous D-LDO regulator with a high frequency clock. A trade-off between voltage tracking speed and current efficiency exists in the clock-triggered synchronous D-LDO regulator design.

III. PROPOSED SYSTEM

In this paper, we propose a new scheme of power-efficient digital linear LDO regulator based on a multibit cyclic TDC for high-level current efficiency, while targeting on driving super-to-near-threshold logic gates [6]. The highly linear VTC circuit is used employing basic current starved inverters. To compensate for the degraded transient performance, we propose a transient response boost technique [1], which detects undershoot/overshoot during transient response, and creates additional asynchronous clocks only during that time. The loop gain is increased to settle down the deviated output voltage. The various blocks employed in the proposed digital LDO regulator are presented in the below sections.

A. Transient-Response Boost Mode (TRBM) Operation

When the load current jumps up from a steady-state condition, Output voltage is instantly dropped, since the current is drawn from load capacitor, which is much faster than adjusting the gate of the power transistor, through the loop response operating at clock frequency. The D-LDO takes over the loop control [1], to correct output voltage after the delay of τ_f , inversely proportional to the closed loop bandwidth. With this property, we need to increase the bandwidth to reduce τ_f , and to reduce the peak undershoot at the same time. This goal can be achieved by increasing the overall size of the pMOS transistors, assuming that all the other loop conditions are kept unchanged. However, it causes the voltage ripple to increase, which is unavoidable in such D-LDO regulators. To solve this tradeoff issue, we employed a gain-boosting technique activated only for the transient period, which is named the transient-response boost mode (TRBM). The TRBM detector monitors the magnitude of the undershoot/overshoot, then it controls our D-LDO to increase the loop gain as needed, if Output voltage

goes beyond a predetermined boundary condition. Once Output voltage is reduced to within the boundary values, the loop gain returns to smaller normal value.

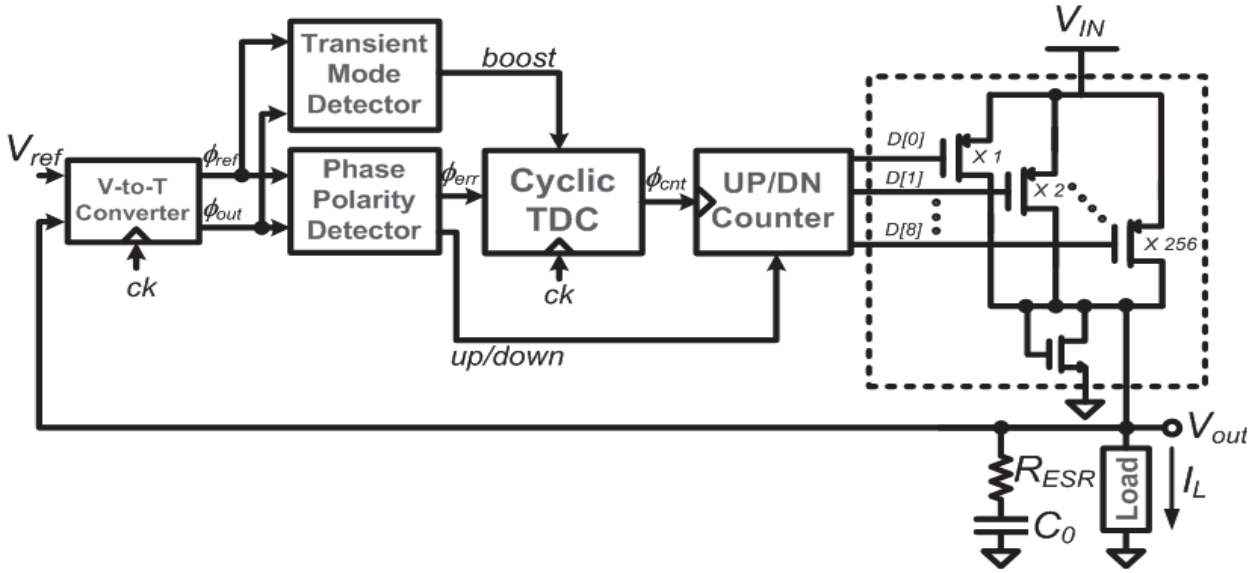

FIGURE 2 BLOCK DIAGRAM OF DIGITAL LDO REGULATOR

B. Voltage to time converter

Time-based ADC is an essential block in designing software radio receivers because it exhibits higher speed and lower power compared to the conventional ADC, especially, at scaled CMOS technologies. In time-based ADCs, the input voltage is first converted to a pulse delay time by using a Voltage-to-Time Converter (VTC) circuit [2], and then the pulse delay time is converted to a digital word by using a Time-to-Digital Converter (TDC) circuit. The VTC achieves high linearity and large dynamic analog input range. A new VTC circuit, based on the current starved inverter architecture, is proposed. The proposed circuit exhibits higher linearity and low power consumption compared to the previously published VTC circuits. The architecture of the proposed VTC circuit [2] is based on the PWM method and achieves high insensitivity to process and temperature variations.

The input clock, VCLK, is applied to the tFALL current starved circuit and accordingly, the voltage V1 is an inverted version of the clock where only the falling delay is controlled by the input voltage. On the other hand, the input clock is applied to an inverted delay line (i.e., odd number of CMOS inverters) and then applied to the tRISE current starved circuit. Accordingly, the voltage V2 is a delayed version of the input clock where the rising delay is controlled by input voltage. The voltages V1 and V2 are applied as inputs to a CMOS XNOR gate that produces the pulse width modulated output voltage, VPWM.

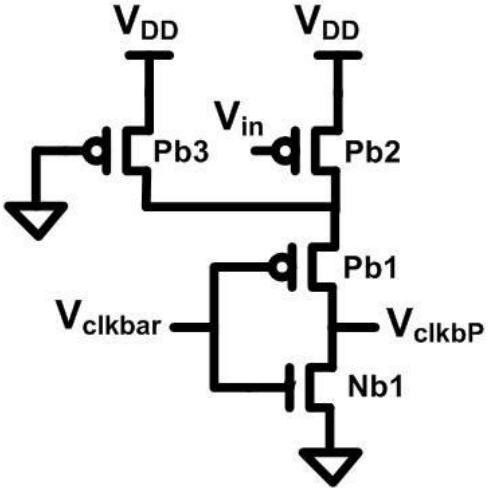

FIGURE 3 t_{RISE} current **STARVED INVERTER CIRCUIT**

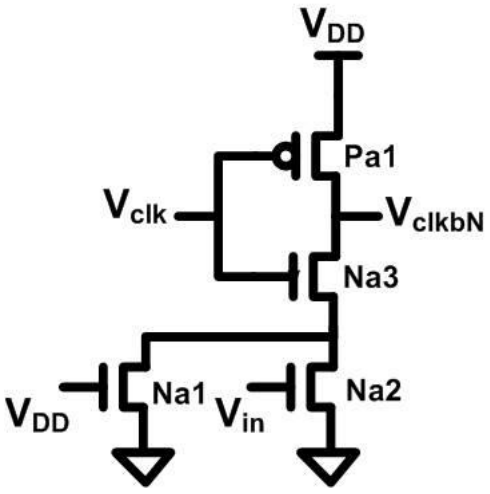

FIGURE 4 t_{FALL} **CURRENT STARVED INVERTER CIRCUIT**

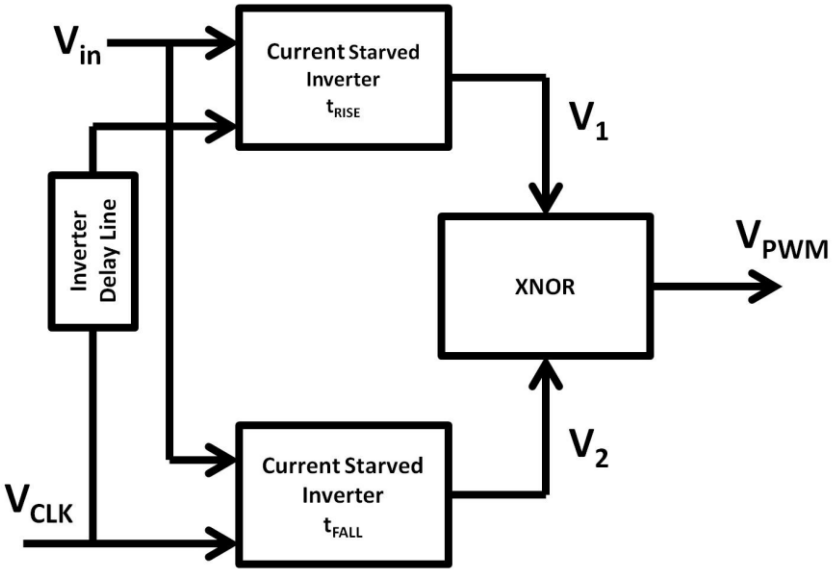

FIGURE 5 BLOCK DIAGRAM OF VTC

C. Phase and polarity detector

A three-state phase-frequency detector (PFD) with polarity detector is as shown below. The PFD is composed of two D flipflops with asynchronous reset, AND, and OR gates. If φref goes to HIGH, while all the D flip-flops keep LOW, Q of DFF0 is raised to HIGH. If this event is followed by a rising transition .on φout, Q of DFF1 goes to HIGH as well, then the AND gate resets both the flip-flops (DFF0 and DFF1) to LOW after the buffer delay of τd , an intentionally made delay, to remove the dead-zone problem in the cyclic TDC. The polarity detector is implemented with a single D flip-flop (DFF2). This circuit discerns the first-coming clock between φref and φout, which represents that the corresponding voltage is lower than the other. As an example, if φref is faster than φout, i.e., Reference voltageis lower than Output voltage, the output of up/down is set to LOW, so that the counter is decremented. The TRBM detector triggers the output (boost) HIGH, when the time difference between φref and φout is increased beyond τD or more, which means that Output voltage deviates from a preset boundary, because of the overshoot/undershoot during the transient response.

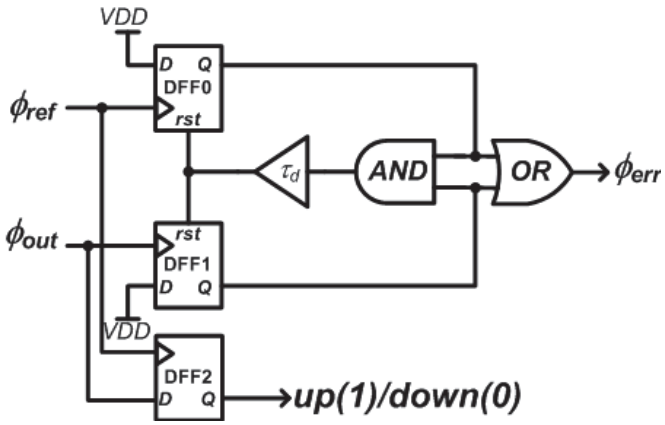

FIGURE 6 PHASE AND POLARITY DETECTOR CIRCUIT

The TRBM detector triggers the output (boost) HIGH, when the time difference between *φ*ref and *φ*out is increased beyond *τD* or more, which means that *V*out deviates from a preset boundary, because of the overshoot/undershoot during the transient response. Once TRBM is entered, the number of pulses in *φ*cnt is multiplied four times, by tapping the nonoverlapped clocks (*D*1, *D*3, *D*5, and *D*7) from the intermediate nodes of the delay chain. This leads to effectively increasing the loop gain by four times, and thus accelerating the loop operation. With this scheme, we can reduce the overshoot/undershoot on *V*out, without any detrimental effect on the ripple after the loop settles down.

IV. CONCLUSION

In this paper, a digital LDO regulator is proposed operated in time domain using a VTC which has high linearity and large dynamic analog input range. The regulator operates in the time domain to achieve higher resolution. The transient response boost technique is employed to reduce the transient response time without increasing the ripples. The loop gain is increased to maintain stable output voltage by transient response boost technique also improves the current efficiency.

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