

Implementation of Quantum Dot Cellular Automata (QCA) Based Logic Circuit in 4-Channel Capacitance to Digital Converter for Capacitive Sensing Solution

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Abstract— The capacitive sensing with grounded capacitor sensor is a very low power, low cost high-resolution contact-less sensing technique that can be applied to a variety of applications ranging from proximity sensing and gesture recognition to material analysis and remote liquid level sensing. As QCA based logic circuits have advantages in simulation time, area, less complexity, etc. It would be possible to get better output in such parameters by using QCA based logic circuits.

Keywords— Capacitive sensing, QCA logic gate.

I. INTRODUCTION

CMOS technology has been the industry standard for implementing VLSI devices for the last two decades and this silicon transistor technology faces challenging problems such as high power consumption and difficulties in feature size reduction. Scaling is another problem of CMOS. To overcome limitations of CMOS technology, emerging nanotechnology called Quantum dot cellular automata (QCA) is the efficient alternative. QCA achieves high device density with extremely low power consumption and high switching speed without using transistors. Fundamental logic primitives of QCA are majority gate, wire and inverter where majority gate output depends on input majority. QCA technology is based on the interaction of bistable QCA cells constructed from nano crystals called quantum dots. Basic gates such as AND, OR, NOT gates can be implemented using majority gate and these basic gates are building blocks of complex circuits. In this paper we have implemented design of 4:1 multiplexer which is used 4-channel capacitance to digital converter using minimum number of cells. This IC has large number of applications such as proximity sensor, gesture recognition, high resolution metal profiling, rain/fog/ice/snow sensor, etc. Design is implemented and simulated using QCA Designer 2.0.3 which gives efficient output.

II. QUANTUM DOT CELLULAR AUTOMATA

Fundamental unit of QCA is quantum dot which is tiny particle of semiconductor materials which has diameter of 2-10nm. QCA cell consists of four quantum dots arranged in corners of cells. Each dot represents a position where an electron can be positioned. Each cell is charged with two free electrons which can tunnel between any of the 4 quantum dots

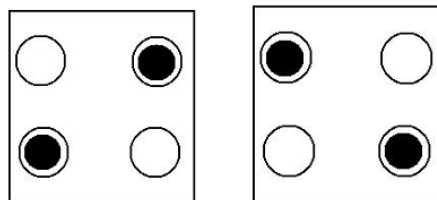


FIG.1: POLARIZATION STATES OF QUANTUM DOT (A) BINARY 1, (B) BINARY 0.

Due to coulomb interaction, the cell charges tend to arrange themselves in order to stay as far apart as possible. The electrons will occupy dots on diagonally opposite sites, making possible to obtain only two states for cell. Here we assume that $p=-1$ represents binary '0' and $p=+1$ represents binary '1' figure 1a and 1b shows the quantum cell.

III. QCA MAJORITY GATE

QCA uses majority gate which has 5 cells, 3 inputs and one output. Its output is majority of the inputs like if 2 inputs are binary '1' then output is '1'. Figure 2 shows majority gate

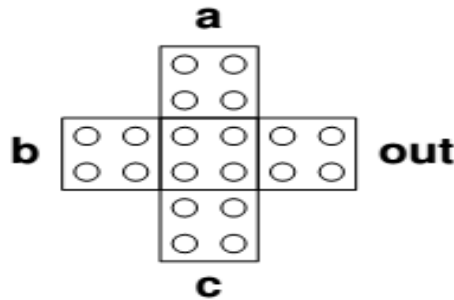


FIG.2 INPUT MAJORITY GATE.

By using majority gate we can design 'OR' and 'AND' gates by fixing polarization as 1 to one of the input for the OR gate and same by fixing polarization as 0 for AND gate as shown in figure.

Fig.3:2-input OR gate and AND gate.

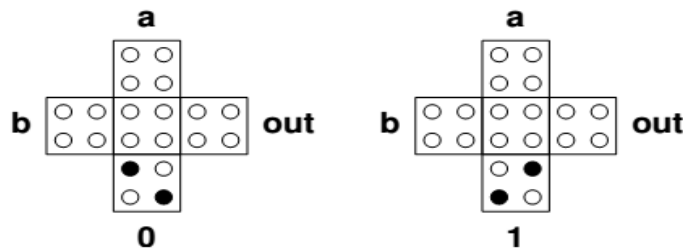


FIG.3-INPUT OR GATE AND AND GATE

IV. DESIGN

4-channel capacitance to digital converter IC can be implemented using QCA and its basic functional diagram is as shown in Fig. 4.

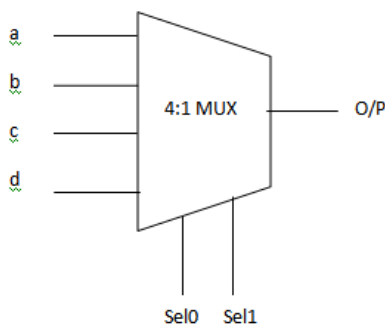


FIG.4: BASIC BLOCK DIAGRAM OF 4:1 MULTIPLEXER

It consists of two select inputs and depending upon these select inputs output is selected and is represented in Table 1. Output function is derived from Table 1 as

$$O/P = Sel0' . Sel1' . a + Sel0 . Sel1' . b + Sel0' . Sel1 . c + Sel0 . Sel1 . d$$

TABLE 1
MULTIPLEXER TRUTH TABLE

Sel0	Sel1	O/P
0	0	a
0	1	b
1	0	c
1	1	d

Using QCAD simulator 4:1 multiplexer is implemented and is better compared to other proposed designs.

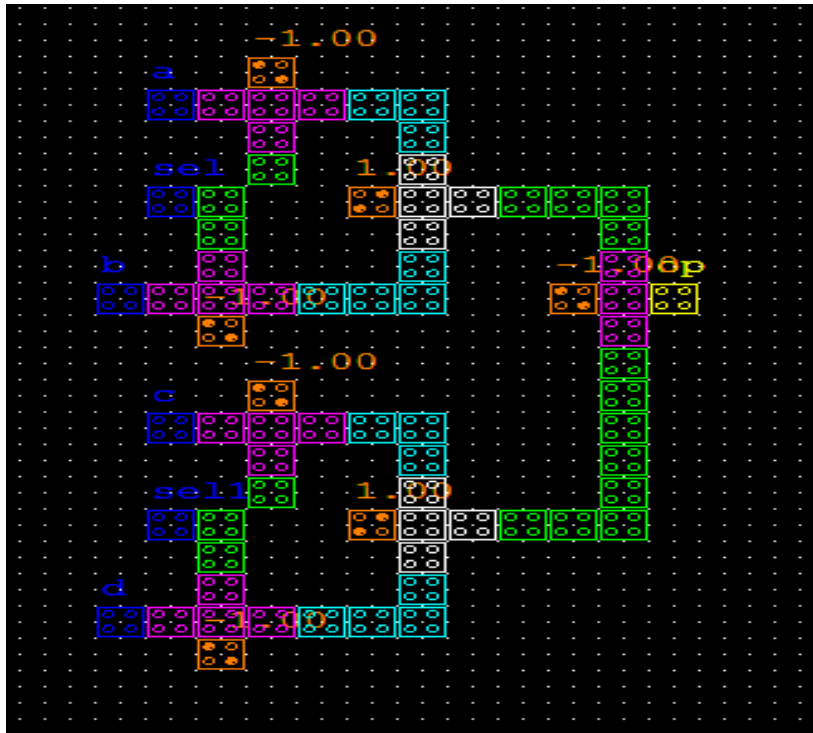


FIG.5: MULTIPLEXER LAYOUT IN QCAD

This can be observed from the Table 2.

TABLE 2
COMPARISON OF PROPOSED DESIGN WITH SOME PREVIOUS DESIGNS

Parameters	4:1 Mux as in article [5]	4:1 Mux as in article [3]	4:1 Mux as in article [4]	Proposed design
No. of cells	95	166	135	73
Area of cells	120204 sq.nm	246404 sq.nm	237244 sq.nm	97844 sq.nm
Cell area	30780 sq.nm	53784 sq.nm	43740 sq.nm	23652 sq.nm
Input to output delay	Seven clock zone	Four clock zone	Five clock zone	Four clock zone

V. SIMULATION RESULTS

Simulation is done using QCAD 2.0.3. The following parameters are used for bistable approximation:

- Cell size=35nm

- Number of samples=60358
- Convergence tolerance=0.00001
- Radius of effect=31nm,
- Relative permittivity=12.9
- Clock high=9.8e-22 J
- Clock low=3.8e-23 J
- Clock amplitude factor=2

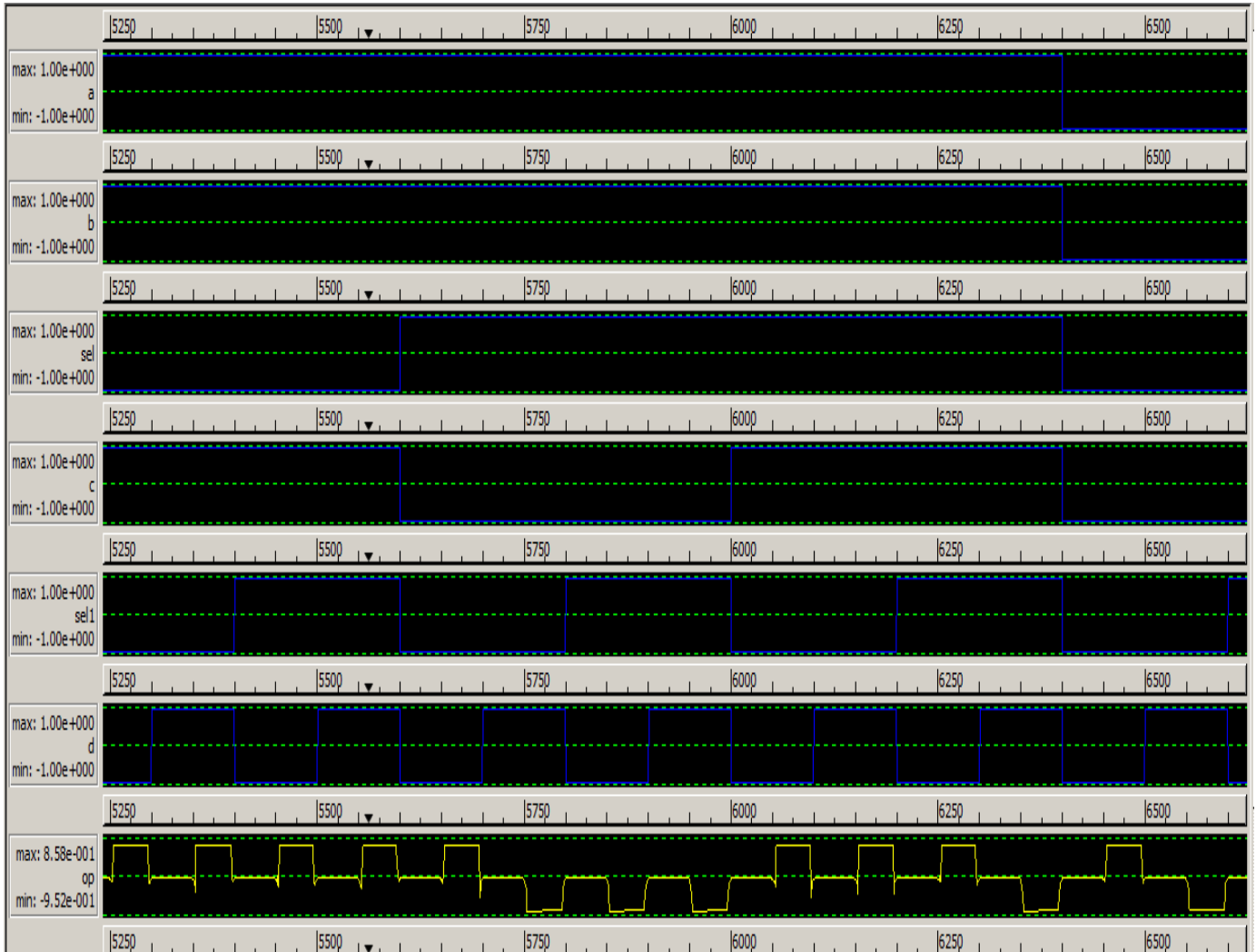


FIG.6: SIMULATION RESULTS OF 4:1 MULTIPLEXER

VI. CONCLUSION

Proposed 4:1 multiplexer is designed and tested using QCAD software. The implementation includes less number of cells and found to be more efficient with reduced cell area compared to other proposed designs. This design can be used for 4-channel capacitance to digital converter which is having number of applications. As design is implemented in QCA, better output can be obtained with high switching speed consuming less power.

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