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VLSI Testing using Matlab Based Cost Modeling

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Abstract— *As per Moore's law, the cost for testing integrated circuits and systems is increasing fast as their complexity is increasing. Cost modelling plays a very major role in decreasing the test cost and time to purchase for the customers. It also gives estimate of overall testing. The available modelling for VLSI Testing with Automatic Test Equipment (ATE) is explained in this paper. The mathematical relations for cost model are developed to test the VLSI circuits based on the available parameters of ATE. Testing is done further for cost modelling equations which are modelled into Graphical User Interface (GUI) in Matlab, which can be used as a general cost estimation tool. A survey is done for Set-top-box, Microprocessor, Device A to verify the reliability of the developed estimation tool. It provides the Test engineers for calculating the testing cost for the test planning.*

Keywords— VLSI Design, VLSI Testing, Cost Modelling, ATE.

I. INTRODUCTION

Test cost is very essential factor for tedious chip designs. As per this generation of System on Chip appears in the industry, the Integrated circuit that was designed usually turns into more complex than the available conventional designs, so the expense of testing is may increase. The cost related to the development of this semiconductor testing algorithms and methods for ATE is the main driving factor. The mathematical modelling equations used to calculate the costs of a product or project are known as cost estimation models. These models are typically important for business plans and tracking mechanisms. The continuing importance focus on cost of the test that will result in a better understanding of cost trade-offs between test methodologies as per ITRS 2007[1] as shown in the figure1. Usually, the cost of test boosts exponentially with an improvement in defects per million (DPM). Parametric modelling in MATLAB GUI (graphic user interface) is very powerful as it decreases the designer's time. Modification of any designed function in MATLAB GUI is very simple. The flexibility of MATLAB is used for quick deployment of the complex software to the end user.

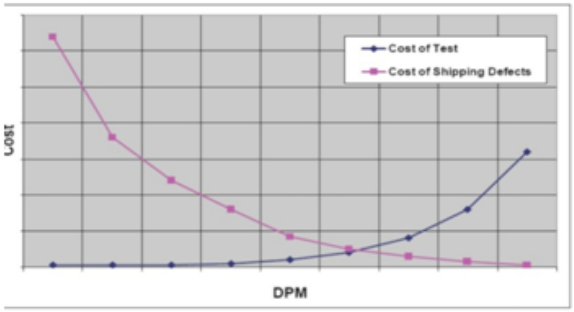

FIGURE 1: QUALITY AND COST TRADE-OFF [ITRS 2007]

The paper is categorized as follows: Section 2 explains the related work of economics of VLSI Testing and cost modelling. Section 3 describes the test cost model that is used for the automatic test equipment for multisite module testing. In Section 4 contains procedure for the cost modelling tool development using Matlab. Section 5 presents a case study three devices for the verification of the economic analysis tool. Section 6 deals with the conclusions

II. RELATED WORK

Many scholars have explained the idea and benefits of the cost of manufacturing test in the past. Some of them are explained here. *Von-Kyoung Kim et. al.3]* described a test cost prediction model which evaluates and optimizes manufacturing test cost.

I.D. Dear et.al. [2] the authors explained the economics of test. The EVEREST test strategy planner tool that is used for the planning of test. *Andrew[4]*developed a Semiconductor Test Economic Model that can simply be applied to decrease overall cost of test and increase throughput. It gives idea to the to the Test Engineers for best decisions on the issues related to: test time reduction, multisite testing, yield, handler index time, ATE Utilization, and ATE Marketing. *Erik et.al[5]* discussed the advantages and tradeoffs by applying them to technical cost modelling on four applications. *Kenneth[6]* gives the estimated the economic uses of the DFT and also suggested that the testability features should not be added to high volume products. *Abadir et* al. [7] developed Hi-TEA, a MCM testing strategy selection tool, which helps to select the cost strategy for the multi-chip module (MCM). Their tool requires cost parameters which include die test cost and wafer yield, that are the parameters difficult to know in the early stage of design. Therefore, their tool may not be practical to analyse a chip testing cost early on.

III. ECONOMIC COST MODELLING FOR ATE BASED VLSI TESTING

The cost of semiconductor test to the organization has many aspects that are labour cost, floor space cost, ATE cost per site etc. The importance of these drivers varies substantially from one device to another. Test development costs are more significant for the products with lower volume. Cost model is structured using the cost parameters figure 2

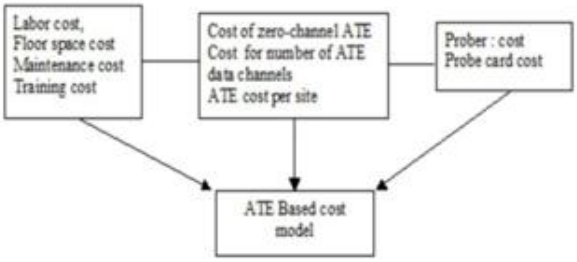

FIGURE 2: ECONOMIC COST MODEL FOR ATE BASED VLSI TESTING

The cost model is targeted for the reduction of the initial equipment cost and the test time. The area increase due to Design for Testability (DFT) implementation is not considered here so silicon capital cost for DFT is not modelled. Therefore, this model assumes only cost associated with spending time on equipment and test engineering. Cost model is used for wafer sorting during testing. One assumption is done here is that all functional tests are done in package test

The cost is calculated as:

$$C_t=C_{cap}*[C_{testcell}.T_{total}/N_{site}]*[N_p.C_p/N-N_{life\text{-}volume}] \quad (1)$$

Where,

Ctest cell : Total capital equipment cost of the test cell,

N*p* : Number of Probe cards

Ttotal : Total time a die spends on the equipment

Ct : Total time of a die spends on the ATE

Nsites : Number of dies tested in parallel.

C*cap* : Constant consist amortization, utilization, labour cost,

floor space, maintenance and training cost.

To calculate Np equation is given as

$$N_P=[N_{life\text{-}volume}/N_{site}*N_{mtd}] \quad (2)$$

Where

Np : No. of probe cards

Nmtd : Maximum touchdowns and

N life-volume: Life time volume of dies

The cost of *Np* probe cards, which cost *Nlifetime-Volume* of the product and maximum touchdowns *Nmtd.* The pseudo code the developed cost model is given below

{Enter the required data from user like

Enter Probe card cost;

Enter number of devices ;}

First of all for the calculation of Nsites

Matlab code is

{Rsignal = .1;

Nsite_ms = str2double (a)/str2double (b);

Nsite_ms_ATE=

str2double(c)/ str2double (d);

if (Nsite_ms< Nsite_ms_ATE)

Nsites_MS = Nsite_ms;

Else(Nsites_MS= Nsite_ms_ATE;)

: end }}{Similarly Matab code is developed to

calculate the total cost Ct}

IV. COST MODELING TOOL WITH MATLAB GRAPHICAL USER INTERFACE

Market modelling and Cost prediction are new areas in which the interest of both physical and the mathematical researchers is increasing due the stochastic nature of the financial processes. Constraining this interest it becomes vital to develop comprehensive software environment, which will use the same models for the reduction of quantitative analysis. The main merit for such approach is that it provides quick prototyping, increased-quality visualization and enhanced model testing to the customers.

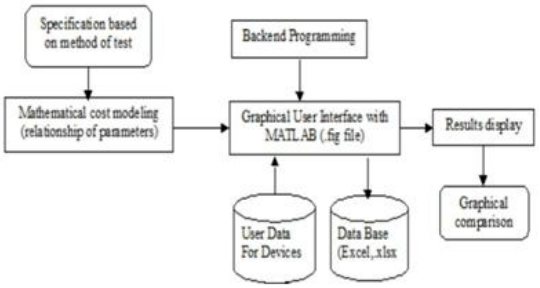

FIGURE 3: TOOL DEVELOPMENT OF COST MODELING

GUI design depends on mathematical expressions and user inputs Graphical User Interface is designed in MATLAB (.fig file) and backend call back functions are known from GUI for each estimation. Development of GUI and also its link along with the database are shown in figure 3. In this, GUI has been generated for mathematical equations. Numbers of input variables are set depending upon the expression to be designed. Property of each single component is set in the Property Inspector. A MATLAB code is written, which is created along the call backs of a particular push button. An event is created by clicking on push button for end result calculations, which affects the function of the button to be executed. A link is established between database which is created in excel file and GUI. The model will help us find the direct cost impacts of various values in the balanced scorecard, for the test processes. Using this cost models, the relative effectiveness of both different test processes can be found .In order to calculate the total cost of every test process user is required to enter all the input data as per parameters required for estimation are shown in the figure 4.

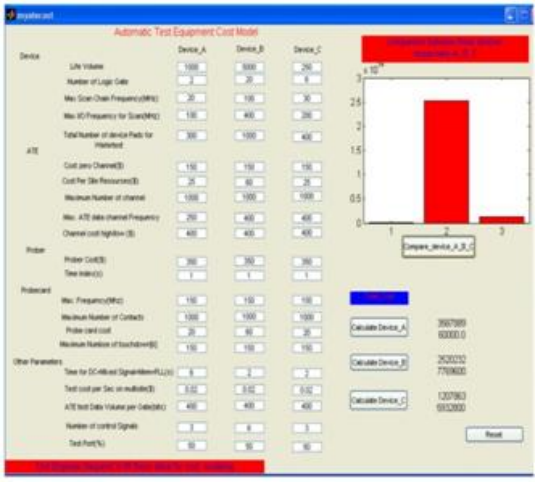

FIGURE 4: A VIEW OF TOOL DEVELOPED FOR VLSI TEST COST BASED ON ATE

V. SURVEY FOR VERIFICATION OF COST MODELING TOOL

In this survey three applications are considered. Datas are taken for testing of developed tool from [5] as shown in Table 1. First device is a Set Top Box (STB) with low complexity of 1 million transistor, second a Microprocessor chip (µP) that contains 5 million of transistor complexity and also having many pin count, Third device "A" is taken with less volume of transistors i.e. 250 K only, that can be tested with one probe card only but more probe cards are necessary for µP IC tests on ATE. This tool explains the individual testing cost of the each devices and comparison of three of various devices is demonstrated graphical form in same GUI.

VI. CONCLUSION

In this paper vlsi testing using matlab based cost modelling is presented. The mathematical expressions are modelled using MATLAB GUI interface in which a Graphical interface are given to the test engineers which is very helpful to save the time in cost calculations and that GUI also verifies the three devices at a time, which will give the accurate estimation for the testing cost in VLSI testing process. This work can be also extended for both DFT and without DFT based cost models in MATLAB for the future scope. For the future scope, we are developing GUI based cost-modelling tool for DFT, BIST, and SOC for standalone systems.

REFERENCES

[1] Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors (ITRS), 2007
[2] Dear, I.D., Dislis, C., Ambler, A.P., Dick, J. Economic effects in design and test, Design & Test of Computers, IEEE, vol.8(4) (1991):64-77

International Journal of Engineering Research & Science (IJOER)
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[3] Kim, V., Chen, T., and Tegethoff, M., ASIC Manufacturing Test Cost Prediction at Early Design Stage. IEEE international Test Conference (1997) 356-61
[4] Andrew C. Evans, Applications of Semiconductor Test Economics, and Multisite Testing to Lower Cost of Test, International Test Conference1999 (ITC'99)
[5] Erik H. Volkerink, Ajay Khoche, Jochen Rivoir, Klaus D. Hilliges, Test Economics for Multi-site Test with Modern Cost Reduction Techniques, 20th IEEE VLSI Test Symposium (2002), 411 – 416
[6] Butler, K. M., Estimating the Economic Benefits of DFT 16th IEEE Design. Test symposium 1999, 71-79
[7] M. Abadir, A. Parikh, L. Bal, P. Sandborn, and C. Murphy,. High Level Test Economics Advisor (Hi-TEA), Journal of Electronic Testing Theory and Practice, vol. 5 (1994), pp. 195–206.
[8] Pranab K. Nag, Anne Gattiker, Sichao Wei, R.D. Blanton, Wojciech Maly, Modeling the Economics of Testing: A DFT Perspective, IEEE Design and Test of Computers, (2002) 19(1): 29-41.
[9] Karthik Sundararaman, Shambhu Upadhyaya, Martin Margala, Cost Model Analysis of DFT Based Fault Tolerant SOC Designs, 5th International Symposium on Quality Electronic Design (ISQED'04), (2004): pp 465-469
[10] W. Radermacher and J. Rivoir, An Evolution to a DFT centric test paradigm that scales with technology progress, Proceeding of European Test Workshop. 2001pp 201-12
[11] Online: http://www.mathworks.com/products/matlab/, website of The Math Works, Inc. developer and distributor of technical computing software Matlab.
[12] Chun-Ming Huang; Chien-Ming Wu; Chih-Cyau Yang; Wei-De Chien; Shih-Lun Chen; Chi-Shi Chen; Jiann-Jenn Wang; Chin-Long Wey; , "Implementation and prototyping of a complex multi-project system-on-achip," Circuits and Systems, ISCAS 2009. IEEE International Symposium on , vol., no., pp.2321-2324, 24-27 May (2009)